Featuring LeCroy's

SDA-PCIE-G2

New Compliance Framework FOR PCI Express Gen1(v1.0a, v1.1) and Gen2 (v0.5)

Operator's Manual

October 2005

LeCroy Corporation

700 Chestnut Ridge Road
Chestnut Ridge, NY 10977–6499
Tel: (845) 578 6020, Fax: (845) 578 5985

Internet: www.lecroy.com

Manufactured under an ISO 9000 Registered Quality Management System

Visit www.lecroy.com to view the certificate.

This electronic product is subject to disposal and recycling regulations that vary by country and region. Many countries prohibit the disposal of waste electronic equipment in standard waste receptacles.

For more information about proper disposal and recycling of your LeCroy product, please visit www.lecroy.com/recycle.

PCIE-G2-OM-E Rev A
913660 Rev A

INTRODUCTION TO SDA-PCIE-G2

The New LeCroy PCI Express Development Software for the SDA 6000A, SDA 6020 and SDA 11000 serial data analyzers is designed with two major objectives in mind:

- First and foremost, SDA-PCIE-G2 provides the necessary tools to develop PCI Express-compliant devices in a systematic, step-by-step fashion, in accordance with the latest standards and specification documents published by PCI-SIG.
- Quick and easy access to all the compliance test requirements from the base and add-in card specifications, and summarized in the Signal Quality Test ("Sigtest") electrical test tool. LeCroy uses the Intel-certified DLL and integrates the tool into the X-Stream processing software, thus enabling in-process measurement and reporting of PCI Express critical parameters.

The standard features of the SDA also provide a broad tool set for advanced debugging of these interfaces, including jitter, eye pattern, and bit error rate.

The New LeCroy PCI Express Development Software (SDA-PCIE-G2) supersedes the LeCroy PCI Express Compliance software (SDA-PCIE). Existing SDA-PCIE users can upgrade to SDA-PCIE-G2 as an option to the SDA 6000A, SDA 6020 and SDA 11000 Serial Data Analyzers by installing version 4.1.1.3 or later of X-Stream DSO firmware.

Required equipment

- SDA 6000A, SDA 6020 or SDA 11000
- PCI Express Compliance & Development software option (LeCroy SDA-PCIE-G2)
- 2 matched-length SMA cables for single-ended tests
- 2 differential probes (D600-type for SDA 6000A or SDA 6020, D11000PS-type for SDA 11000)
- 1 SMA T connector
- 1 BNC-to-SMA adapter
- 1 compliance test fixture (CLB or CBB as appropriate for testing a system or add-in card)
- A Host computer, though not required, is highly recommended to execute X-Replay, the Compliance & Development Software Engine.

Additionally, SDA-PCIE-G2 takes advantage of LeCroy's full line of PCI Express Protocol tools in order to force the DUT to enter or abandon a particular State for the purpose of making amplitude or timing measurements. These tools are used for SDA-PCIE-G2 implementation. LeCroy recommends the use of the following tools:

- PE Tracer (PCI Express Protocol Analyzer)
- PE Trainer (PCI Express Protocol Exerciser)
- PE Host Emulator (PCI Express System Board with x8 slot)

For an example featuring the above protocol tools, refer to ***Appendix A*** section of this manual. Specific instructions on how to use LeCroy's protocol tools can be found at www.lecroy.com

PCI Express Compliance Test Fixtures

The PCI Express standard describes a set of two fixtures that are used to connect to the signal under test. The fixtures are known as the compliance load board (CLB) and the compliance base board (CBB). The CLB is used to test system boards, and the CBB is used for testing add-in cards. Both the compliance load board and compliance base board are available through the PCI special interest group (PCI-SIG) at www.pci-sig.org

Using SMA type cables, both fixtures allow for the attachment of the positive and negative lines of the differential signals directly to separate channels on the instrument. The 50 ohm impedance on each oscilloscope channel provides the proper loading for compliance testing. All PCI Express add-in cards and system boards must transmit a standard compliance pattern when loaded with 50 ohms to ground on each line, at the same time that no signal is being received. The fixtures are designed to apply the compliance test load to the ports of the device under test. The CBB also has a socket for a standard ATX power supply and a 100 MHz system clock that is used by add-in

cards plugged into the fixture. Please note that effective May 2005, a CBB compliant with Version 1.1 of PCI Express Base Specification is also available from PCI-SIG. See Figure 3.

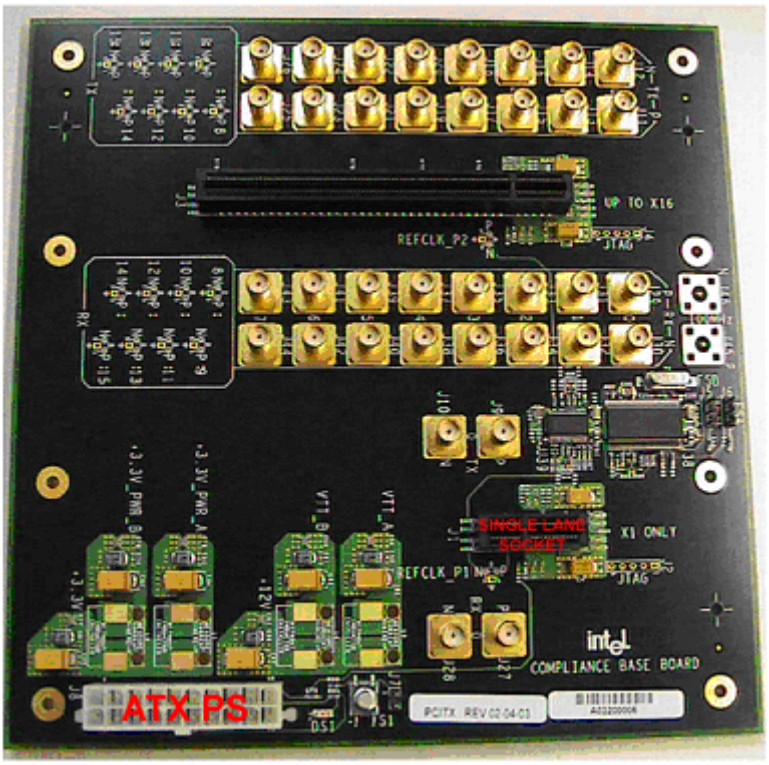


Figure 1. Compliance base board (CBB) provides sockets for 1 lane and 16 lane add-in cards. The SMA jacks allow access to the D^+ and D^- signals from the connectors. The ATX power supply connection is at the bottom edge of the board and the clock is just above the single lane socket.

Figure 2. The compliance load board (CLB) connected to a motherboard. This fixture provides probing access for 1, 4, 8, and 16 lane connectors. This figure shows the 1 lane section being used. The SMA cables connect the D^+ and D^- signals to the oscilloscope channels.

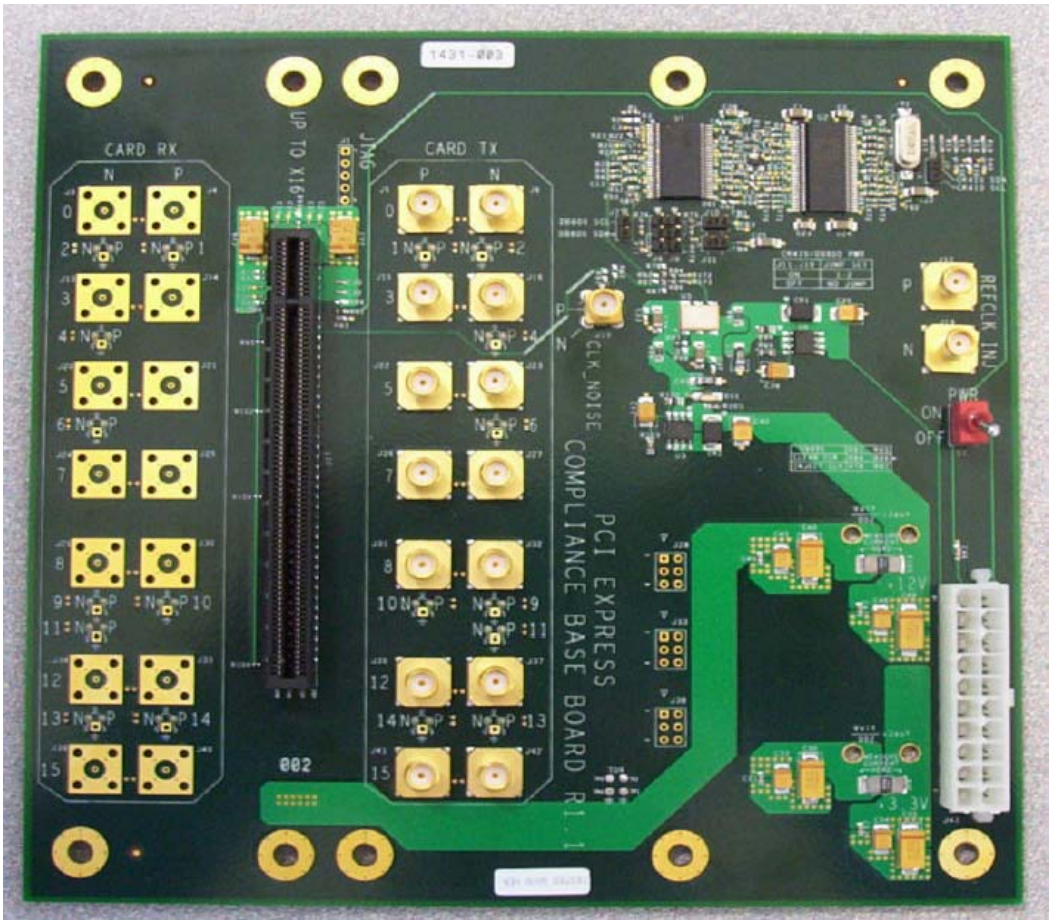


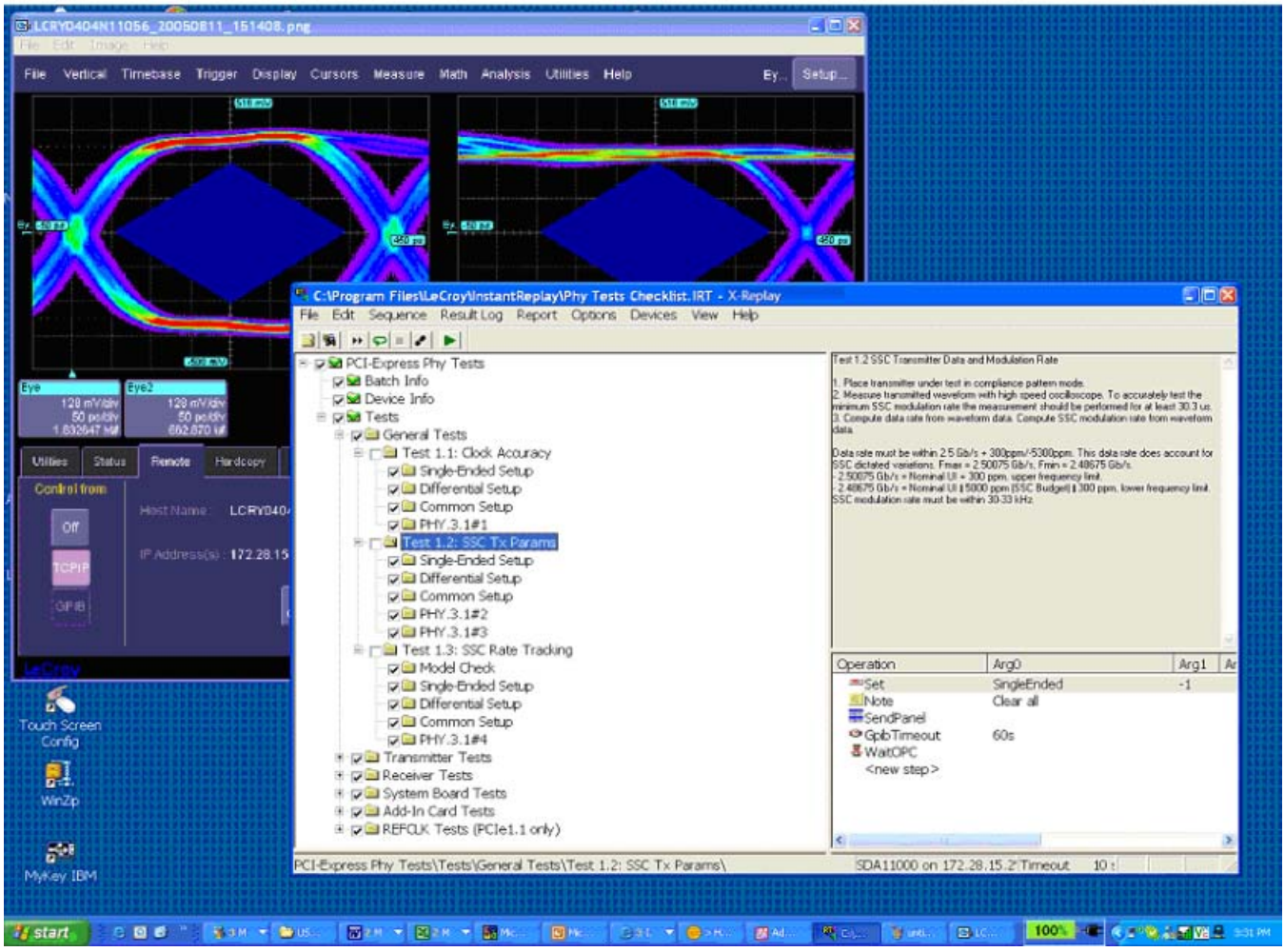
Figure 3. New Compliance base board (CBB) for version 1.1 provides a clean reference clock and clock noise injection capabilities.

SOFTWARE INSTALLATION AND SYSTEM CONFIGURATION

What Is X-Replay?

The new PCI Express Software application incorporates X-Replay, a unique application framework. X-Replay is a MS Windows-based application that contains all the commands and instructions necessary to configure, acquire, display, and report measurement results. For instance, X-Replay environment enables you to:

- Create or change test criteria in order to make context-sensitive parametric measurements.
- Export all test results as XML for import into a database program such as Microsoft Access for further manipulation.
- Generate reports from within X-Replay showing the latest test results. Reports are html, i.e., meant to be viewed with Microsoft Internet Explorer.



The PCI Express Compliance software resides in X-Stream DSO software in the scope, and it is activated through the use of an alphanumeric code matched to the scope's serial number. This code is unique to each scope serial number and is activated when ordering SDA-PCIE-G2 software.

While the software key enables the scope to perform the measurements, X-Replay contains the PCI Express script, the test results database and the report generation engine. For ultimate flexibility, X-Replay can be executed from a host computer at a location different from the scope, provided that there is a Windows-compatible network connection.

Option Key Installation

When ordered as an option to a new instrument, no installation is necessary. Installation is required, however, when the option is ordered after the oscilloscope is purchased. An option key will be issued at the time the option is purchased.

To enter the option key code,

1. Touch **Utilities** in the menu bar, then **Utilities Setup…** in the drop-down menu.
2. Select the **Options** tab from the Utilities dialog.
3. In the **Options** dialog, touch the **Add Key** button and enter the option key in the dialog box using the on-screen keyboard.

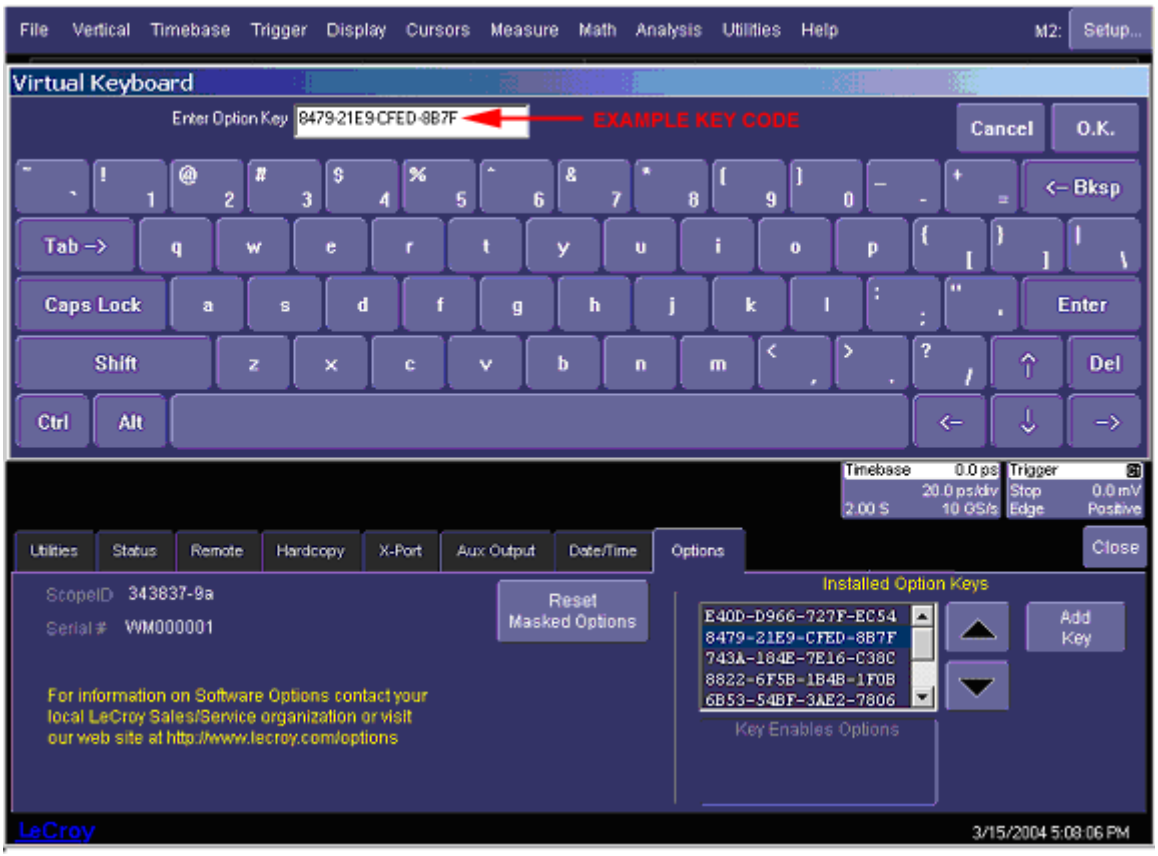


Figure 4. Entering the option key code for the SDA-PCIE-G2 software option

CD-ROM Installation

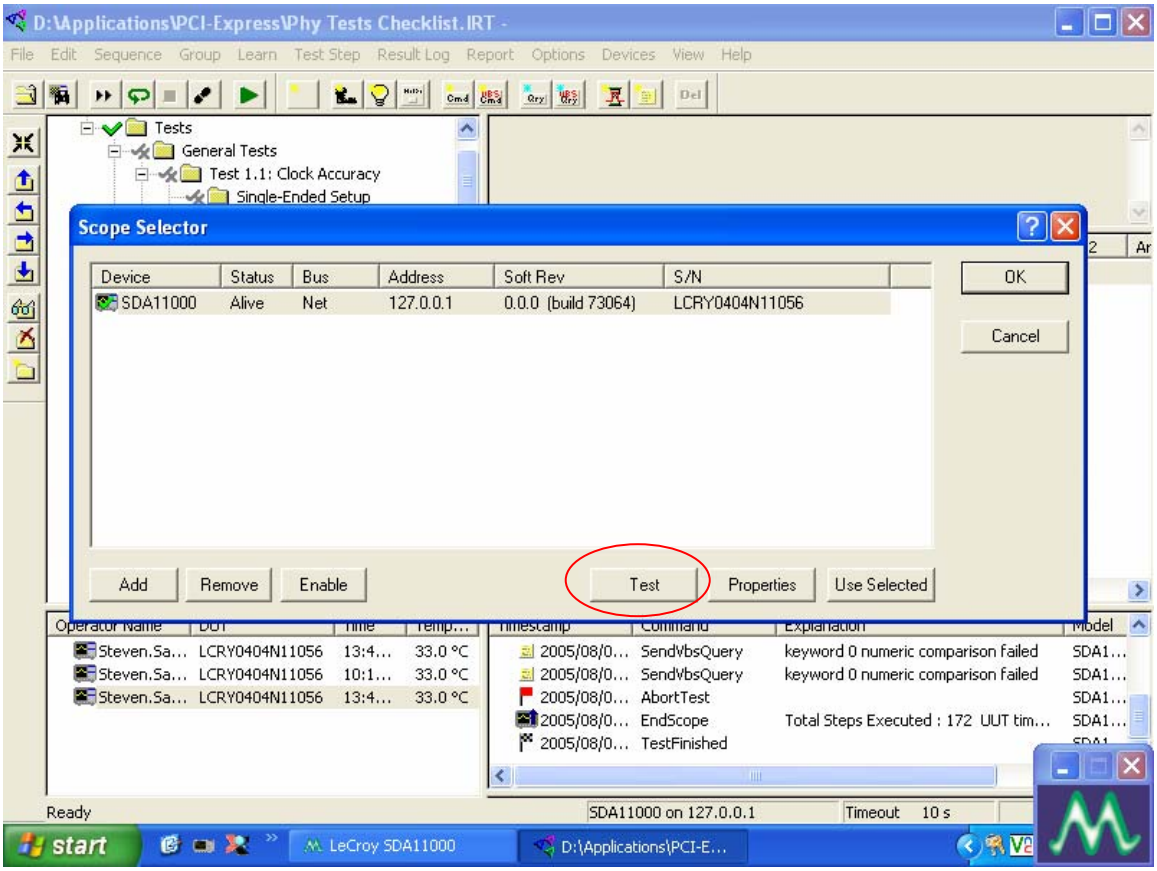
When ordered as an upgrade to an existing SDA-PCIE option, an Application Software CD-ROM is supplied containing X-Replay and other software installation files. Follow the specific instructions in the Installer application. The installation process will prompt you, as required, for specific location of data files and test results, reports, scripts, etc.

Typical (Recommended) Configuration

SDA-PCIE-G2 software can be executed from the scope PC or from a Host PC. By default, a new scope will come equipped with X-Replay installed in the scope. LeCroy recommends that you run SDA-PCIE-G2 in a scope equipped with Dual Monitor Display capability (option DMD-1), such that the waveform and measurements are displayed on the scope LCD display, whereas the X-Replay application and test results are displayed on a second

monitor. By default, the scope appears as a local host (IP address is 127.0.0.1) when X-Replay is running in the scope computer. To verify its correct operation, the following steps must be taken once the scope is turned on:

1. Minimize the X-Stream DSO window.
2. Run X-Replay.
3. Select **Scope Manager**. The scope selector window should display the scope attached (in this case, an SDA 11000)
4. Press the **Test** button. A message box will indicate that the test is OK. X-Replay is now ready for use.

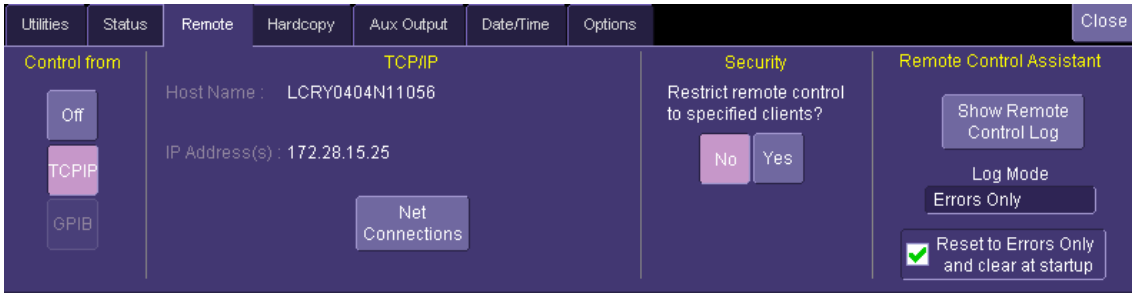


Remote (Networked) Configuration

Of course, it is also possible to run SDA-PCIE-G2 by installing X-Replay in a host PC, controlling the scope through a Windows Network / LAN Connection. This may allow you to run other instruments or applications from the host PC, for example setting up and configuring the LeCroy PE Protocol and Host Emulator instruments. The scope must already be configured and an IP address (fixed or network-assigned) must already be established.

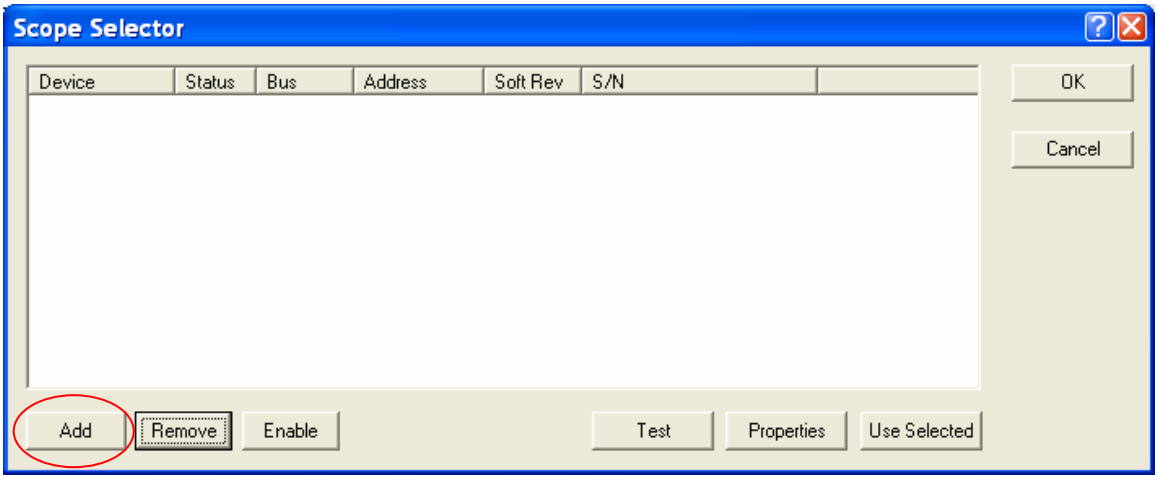
Follow these example steps to set up the scope using X-Replay over a LAN:

1. In the scope, verify in the **Utilities → Remote** dialog that the scope has an IP address, control is set to TCP/IP as shown below:

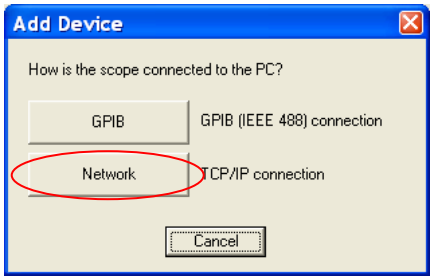


2. Make sure that the host PC is connected to the same LAN as the scope. If unsure, contact your system administrator.

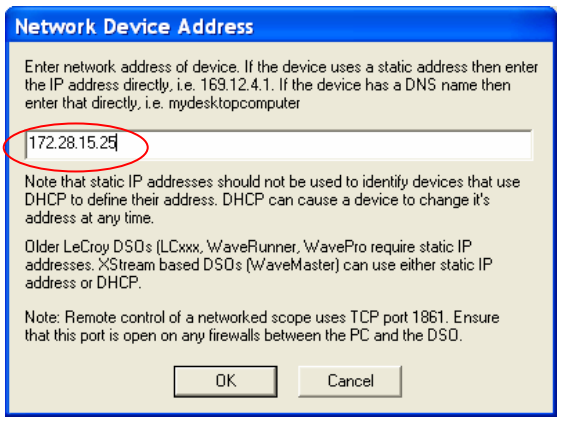
3. Run X-Replay in the host PC and select the **Devices** menu, then **Scope Selector**. The screen will show no devices enabled at this time. Click the **Add** button:



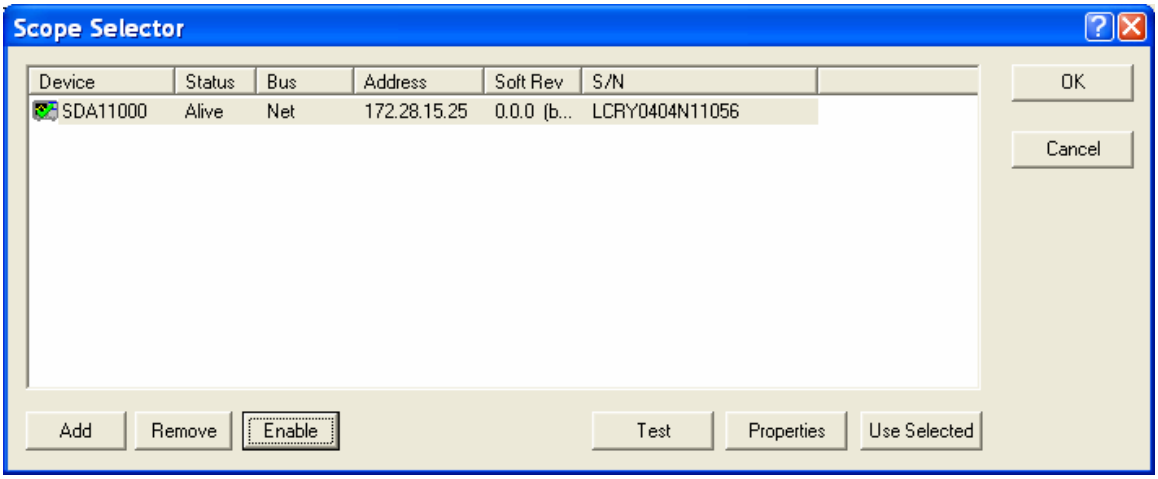
4. Select **Network** as the connection method:



5. Enter the IP address from step #1



6. Click **OK**. The Scope Selector window displays the correct information about the scope connected to the LAN. In our example, an SDA 11000 is connected, as shown below:



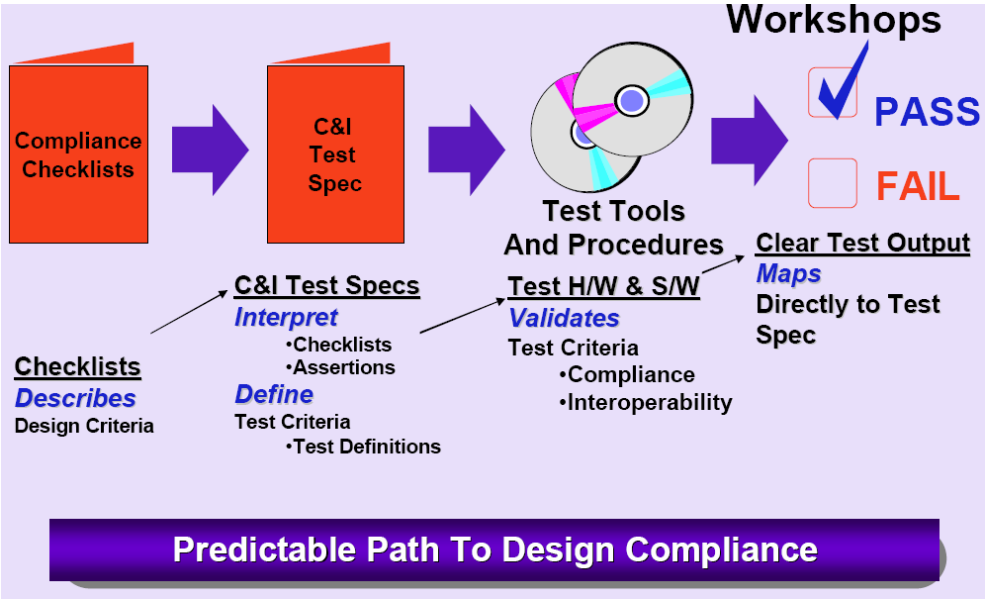
INTRODUCTION TO PCI-EXPRESS

PCI Express is a serial version of the commonly used PCI bus designed for PC's and servers. This serial interface adds scalability through the use of multiple lanes, and flexibility through such features as switching. PCI Express is a multi-lane interface that operates at a signaling rate of 2.5 Gb/s on each lane. The differential signal contains both normal and inverted signal lines designated D^+ and D^-, and the signaling voltages are nominally 800 mV peak-to-peak.

PCI Express is designed to operate on standard PC motherboards using low-cost PCI-type sockets. This implies several things about the signal characteristics. First, spread spectrum clocking must be supported to control emissions in desktop applications. Second, because standard PC motherboards must be used, the signal is pre-emphasized to control inter-symbol interference. Finally, many implementations of serial data receivers employ an "over sampling" mode that takes many samples per bit to find the data transitions rather than using a recovered clock for this purpose.

PCI Express Device Development Process

With the introduction of PCI Express Gen2 in Spring 2005, High Speed PCI Express has arrived. As a result, PCI Express standards are quickly evolving to allow existing Gen 1 (2.5 Gb/sec) designs to interact with the new, demanding 5 Gb/sec requirements. New requirements for PCI Express Gen1 are now identified in the new PCIE Version 1.1 specification, effective April 2005. PCI-SIG encourages new and experienced electrical interface designers to undertake new designs using a "Predictable Path to Design Compliance."



PCI Express Device Development Process and Compliance Tests

The PCI Express **Compliance** test requirements are derived from the test specification document, which is interpreted from the design checklist. The design checklist is a set of requirements that must all be met during the design phase of a PCI Express-compliant device. An example of a few requirements from the design checklist is shown below:

PHY.2.6#1	Training sequence ordered-sets are never scrambled but always 8b/10b encoded.	yes ___ no___
PHY.3.1#25	The receiver terminations must remain enabled in Electrical Idle.	yes ___ no___
PHY.3.2#5	The Beacon signal must contain minimum width pulses >= 2 ns.	yes ___ no___

Figure 5. Example requirements from the PCI Express design checklist

The test specification / Electrical Design Considerations contains a list of **Assertions** that are derived from the checklist. For example, the symbol rate must be 2.5 Gb/s +/-300 ppm. Each assertion has a specific measurement that is used to verify it, the **Test Number**. While there are many tests in the specification, only the signal quality test is performed for **Compliance**.

The new LeCroy PCI Express software supports the measurement of PCI Express signals in two modes of operation:

- ***Compliance Test Mode***, or signal quality test, based on Intel's sigtest dynamically linked library (dll) and used for test and evaluation at PCI-SIG sponsored electrical test workshops. These tests are covered in the Electrical Design Considerations document under Tests 1.4 and 1.5, and can be accessed by manual control on the DSO or by selecting the corresponding tests under X-Replay.
- ***Checklist Test Mode, or Designers Checklist Mode***. In this case, the X-Replay script provides capabilities to run all the test steps required or some group of tests, as many times as specified, and in accordance with the form factor (Add-In card, System card) supported by the device under development. For example, a developer may only be interested in the Tx performance of the chipset, then only the Transmitter Tests are selected for verification.

PCI EXPRESS MEASUREMENT THEORY

Eye Pattern and Jitter Measurements

PCI Express signal quality tests are performed using eye pattern analysis. The eye pattern allows measurement of voltage and jitter. The measurement methodology that has been adopted for eye patterns in this standard is designed to accommodate the requirements of over-sampling detectors and spread spectrum clocking. The method relies on the acquisition of consecutive unit intervals of the data stream sampled at a minimum rate of 20 GS/s.

Version 1.0a Measurements

The average symbol period is measured over 3500 unit intervals (UI). This value is then used to create an eye pattern over a segment of 250 unit intervals in the center of the 3500 UI window. The eye pattern is generated by dividing the 250 UI segment into equal-length segments set by the measured average symbol period. The 250 UI segment is chosen to encompass the range in which over-sampling detectors are affected by jitter. The 3500 UI window is chosen to provide the most accurate symbol period measurement while being minimally affected by any spread spectrum clock that may be on the signal.

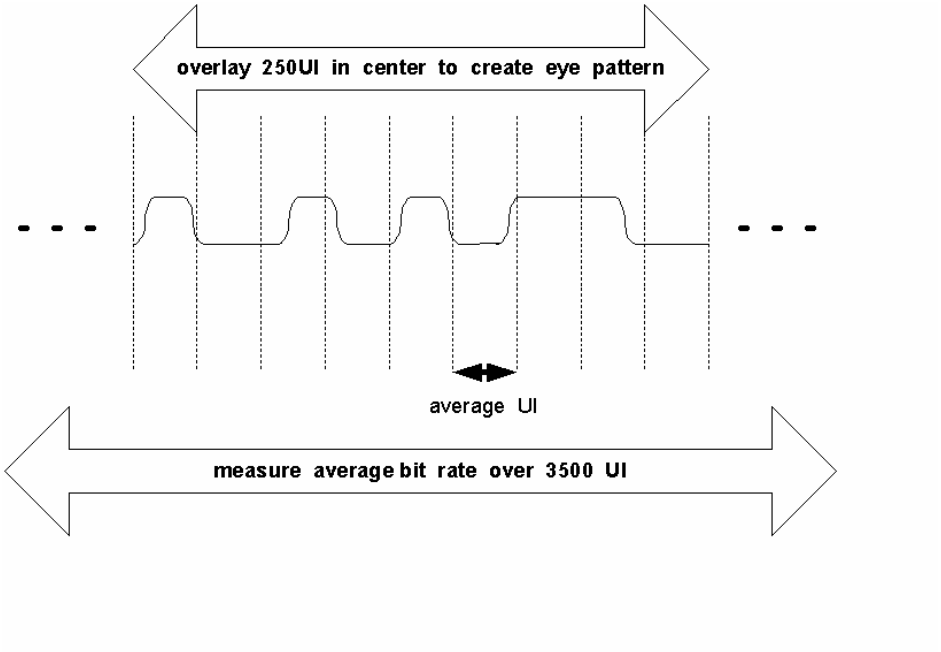


Figure 6. Compliance eye pattern creation (version 1.0a). The eye pattern is created by dividing the center 250 UI of the waveform into segments that are the width of the average UI measured over 3500 unit intervals.

The eye pattern is produced by dividing the 250 UI segment into segments that are 1 nominal UI long. The nominal UI for a given 250 UI segment is measured by finding the median value over a 3500 UI segment whose center 250 UI contain the measurement window. The 1 UI segments are overlain by lining up the median UI boundaries. The median UI was chosen in the standard rather than the average because the median value is more accurate in the presence of low-frequency jitter, such as that caused by spread spectrum clocking.

Version 1.1 Measurements

The revised version of the specification places a premium on the acquisition record size requirements: 1 million UI, which translates to 8 Mpts acquisition record size when running at 20 GS/s. The reference clock is assumed to have been cleaned, i.e., contributes zero jitter:

“The TTX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2 of the PCI Express Base Specification. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is

approximately equal, as opposed to the averaged time value. This parameter is measured with the equivalent of a zero-jitter reference clock. The TTX-EYE measurement is to be met at the target bit error rate. The TTX-EYE-MEDIAN-to-MAX-JITTER is to be met using the compliance pattern at a sample size of 1,000,000 UI." The new clock recovery applies a first order high-pass filter with a -3 dB cutoff frequency of 1.5 MHz, rolling off at -20 dB/decade.

In addition, the new clock recovery function will apply to devices (for example, Add-in cards) that rely on a clean clock. For System board designers, however, the burden of proving that the reference clock is a clean clock is a NEW requirement for PCIE Version 1.1 compliant designs.

PREPARING TO MAKE PCI EXPRESS MEASUREMENTS

Channel Deskew (SMA Cables)

PCI Express signals are properly probed using two separate channels on the oscilloscope connected to the appropriate SMA jacks on the test fixture. The highest measurement accuracy is achieved when the timing skew between the two channels is calibrated. This is performed using the “Deskew” control on one of the two channels to which the differential signal is connected, as follows:

1. Attach the calibrator signal to both input channels using a T connector to rout the calibrator signal on the SDA front panel through the same cables that will be connected to the fixture.

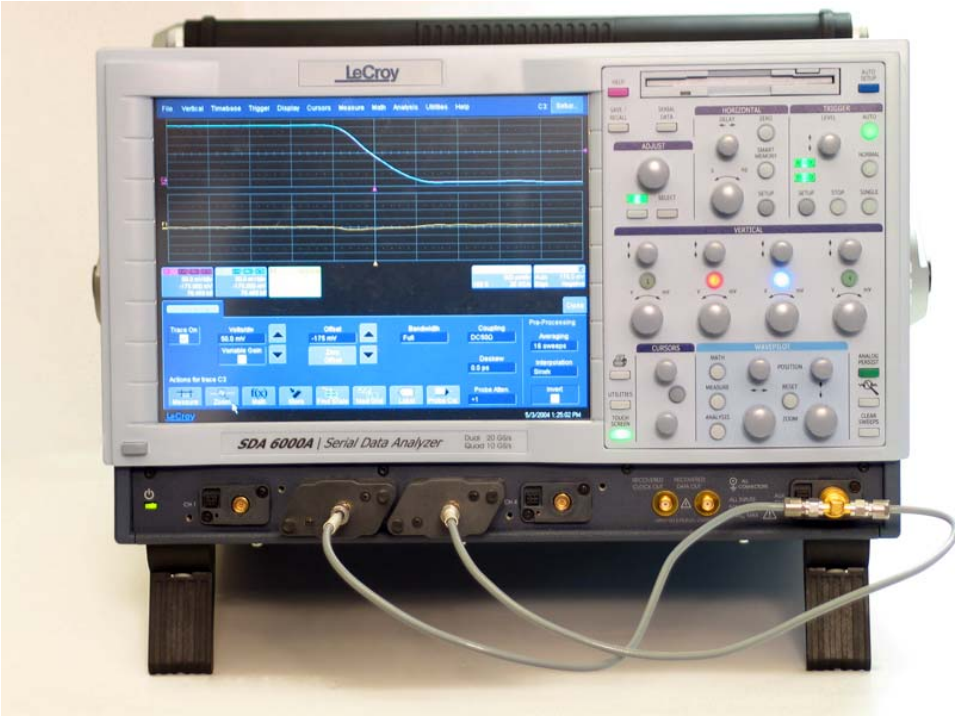


Figure 7. Deskew cable setup. The calibrator signal is connected to the cables using a T connector or resistive divider. The calibrator peak voltage should be set to the same value as the nominal voltage of D^+ and D^-.

2. Set interpolation of both channels to **Sin(x)/x**, using the **Interpolation** control in the **Vertical Adjust** dialog for each channel.
3. Check the **Invert** checkbox on one channel.

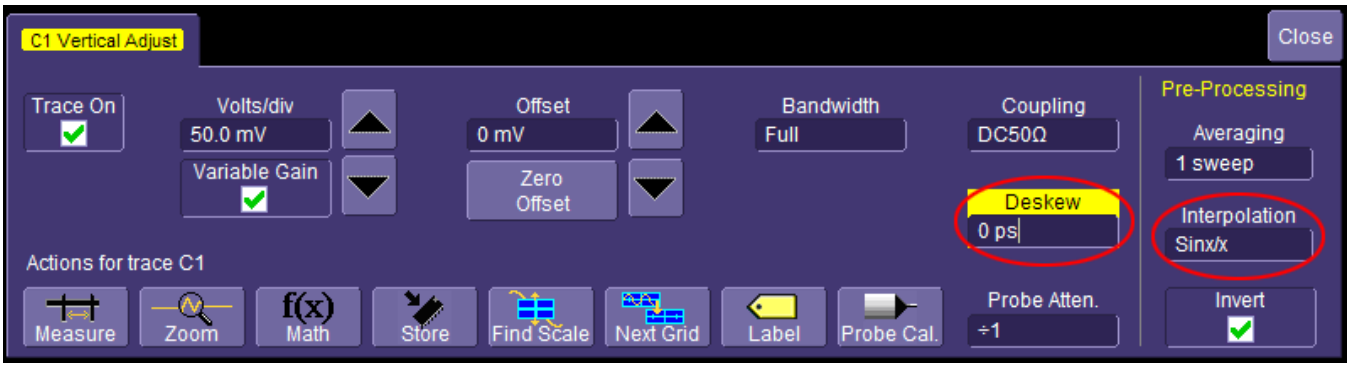


Figure 8. Deskew control in channel menu. Adjust this value to achieve minimum skew.

4. Create a Difference math waveform by selecting **Math** in the menu bar, then **Math Setup…** in the drop-down menu. Touch the "Operator1" field and select **Difference** from the **Select Math Operator** menu. Enter the channels to which your signal is connected in the **Source1** and **Source2** fields. The math function is thus defined as the difference between the 2 channels probing the D^+ and D^- signals.

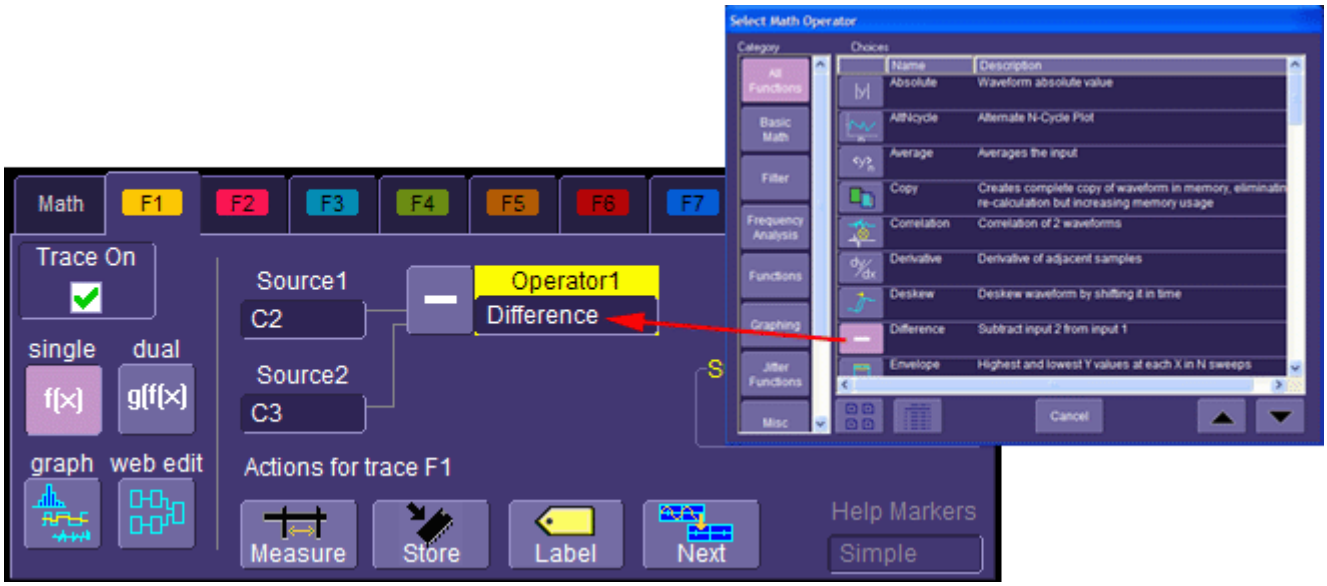


Figure 9. Math setup

5. While viewing the math trace, adjust the **Deskew** control in one of the channels until the math trace is as flat as possible.

Note: With the **Deskew** control highlighted, you can use the front panel adjust knob to make the adjustment.

The best accuracy is achieved by setting the level of the calibrator signal to match the expected levels of the signal under test, and with the calibrator set to its maximum frequency (5 MHz). The calibrator settings can be found in **Utilities → Aux Output**.

Differential Probe Calibration

The PCI Express signal can be applied to a single channel of the SDA using a differential probe, or directly to two channels using one of the test fixtures described above. In either case, the signal level should be maximized on the instrument to achieve the best overall accuracy. The signal level is set in the **Vertical Adjust** dialog, or by using the front panel knobs. The best peaking can be achieved by checking the **Variable Gain** checkbox, which allows finer gain steps in the control knobs.

With the introduction of the 40 GS/s, 2 channel, 11 GHz BW (20 GS/s, 4 channel , 6 GHz) scope with Digital Bandwidth Interleaving (DBI), high-speed PCI Express Gen 2 measurements can now be accomplished. Additionally, the use of two D11000 probes enables the measurement of inter-lane skew on the DBI-enabled channels.

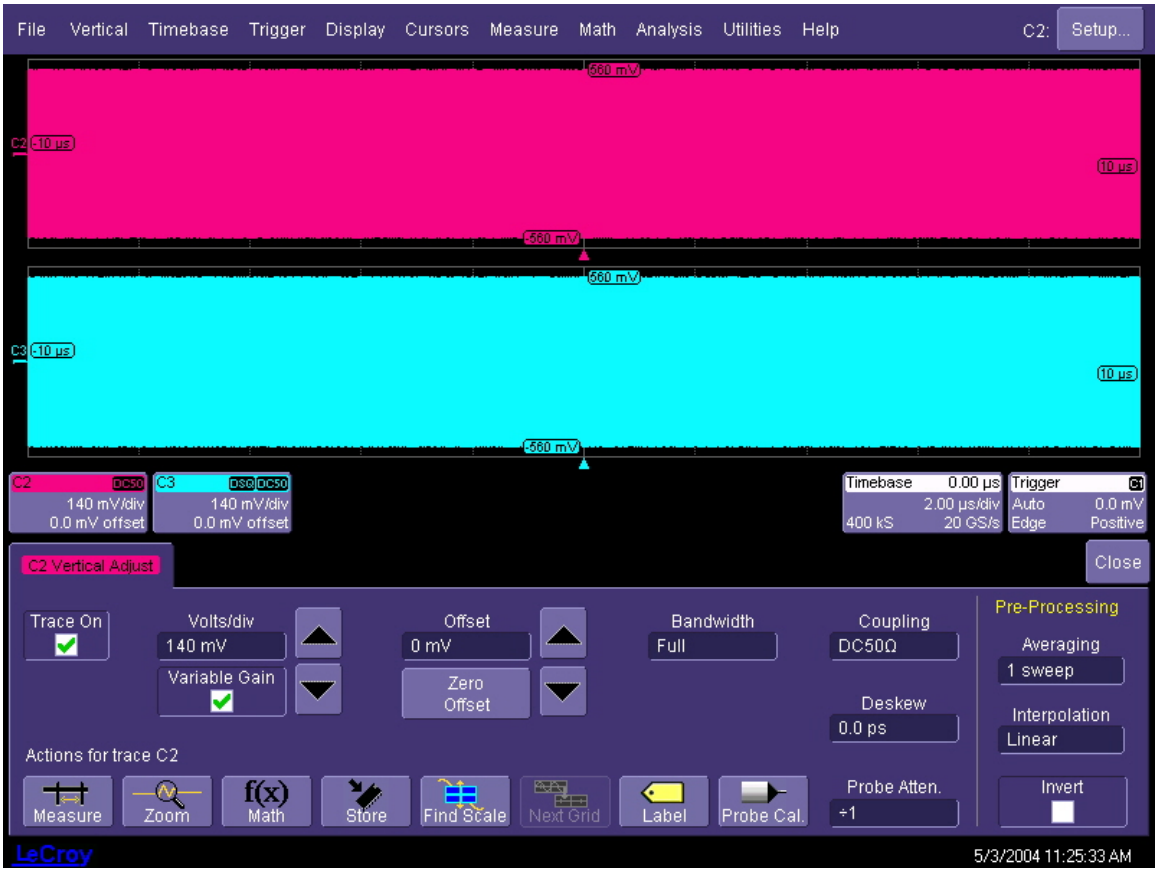


Figure 10. Signals properly adjusted for best accuracy. The signal levels should be adjusted in the "Vertical Adjust" dialog so that at least 6 vertical divisions are filled.

For SDA 6000A

The horizontal scale should be set to a fixed sampling rate of 20 GS/s. This requires that **Auto** or **2** channels be selected in the **Active Channels** control in the **Horizontal** (Timebase) dialog. The record length should be set to a minimum of 8 MS using the **Time/Division** control or the front panel horizontal scale knob. Longer records give more accurate results but also take more time to compute.

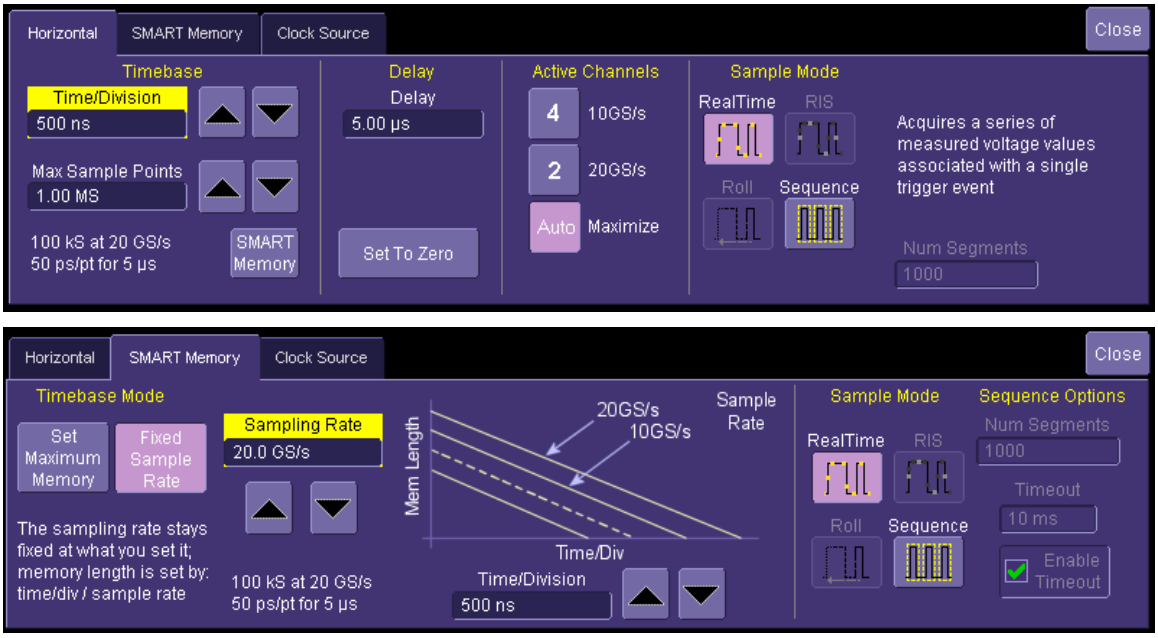
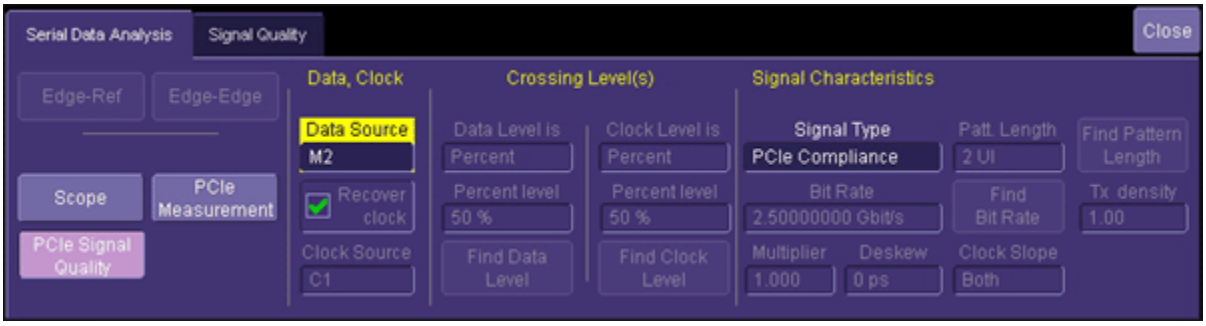


Figure 11. Horizontal and memory setup menus properly configured for testing PCI Express signals. The maximum (20 GS/s) sampling rate must be used. The SDA6020 model does not have the "Active Channels" control since all channels sample at 20 GS/s.

The signal under test is selected from the **Data Source** menu in the **Serial Data Analysis** main dialog. The source can be any channel, memory, or math trace. If a differential probe is being used to couple the signal to the instrument, the channel to which the probe is attached should be entered into the **Data Source** control. When probing with 2 channels of the instrument attached to a compliance test fixture, a math trace should be defined as the difference between the channel connected to the D^+ and the channel connected to the D^- lines on the fixture. The channels should be deskewed as described above.

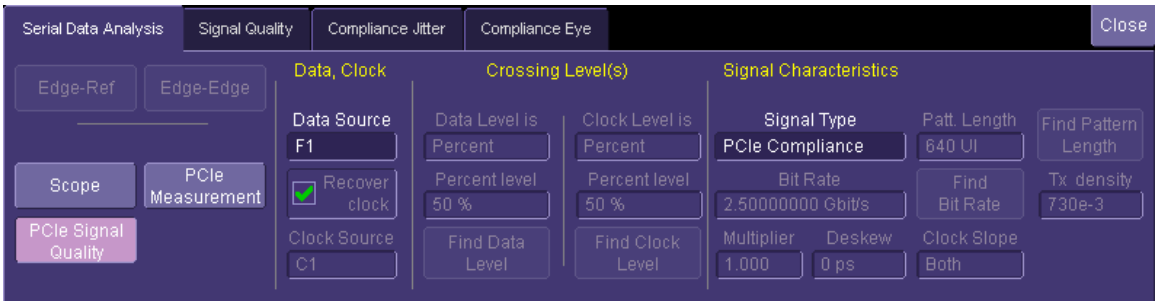
It is also possible to perform measurements on waveform files stored in memory. either on the system hard disk or in non-volatile memory. Subtract the memory traces if they are stored as separate (+ and -) waveforms, as described above, or enter the memory into the **Data Source** control directly.



COMPLIANCE TEST MODE

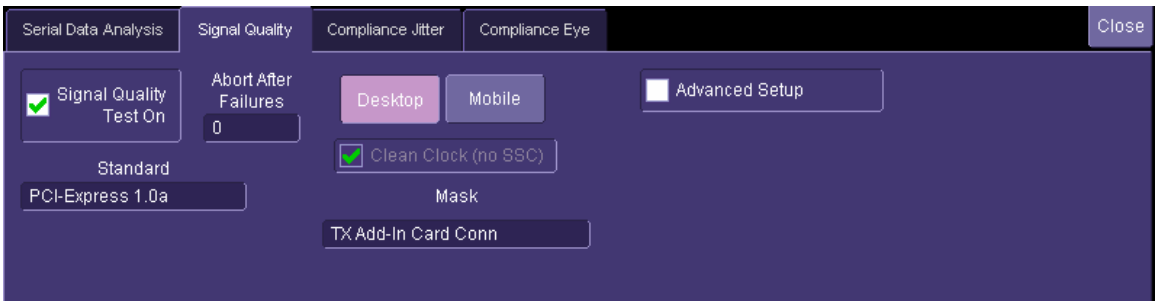
This section describes how to execute the “PCIe Compliance” test built into the SDA, from the SDA’s user interface. Information about using X-Replay to automatically run tests is in the section titled “Checklist Test”, below.

To select the compliance test mode, from Serial Data Analysis menu select “PCIe Compliance” for Signal Type. The following menu appears:



Performing a Compliance Test – PCIe Signal Quality

Compliance testing is defined by the PCI-SIG (PCI Special Interest Group) as consisting of a pair of eye pattern template tests and a set of jitter measurements derived from the eye pattern zero crossings. Compliance testing also includes measurement of the bit (data) rate, bit period (or UI), and voltage levels. Select the **Signal Quality** tab; the following dialog is now displayed:



A compliance measurement is started when the **Signal Quality Test On** checkbox is checked. The compliance test will start and messages indicating the start and completion of the test will be displayed on the bottom left edge of the instrument display. Two eye patterns are displayed in the upper half of the display when the test is complete. The one on the left shows the waveform for transition sections of the trace, while the one on the right shows the non-transition eyes (see the figure below).

First, the form factor (**Desktop** or **Mobile**) button is chosen:

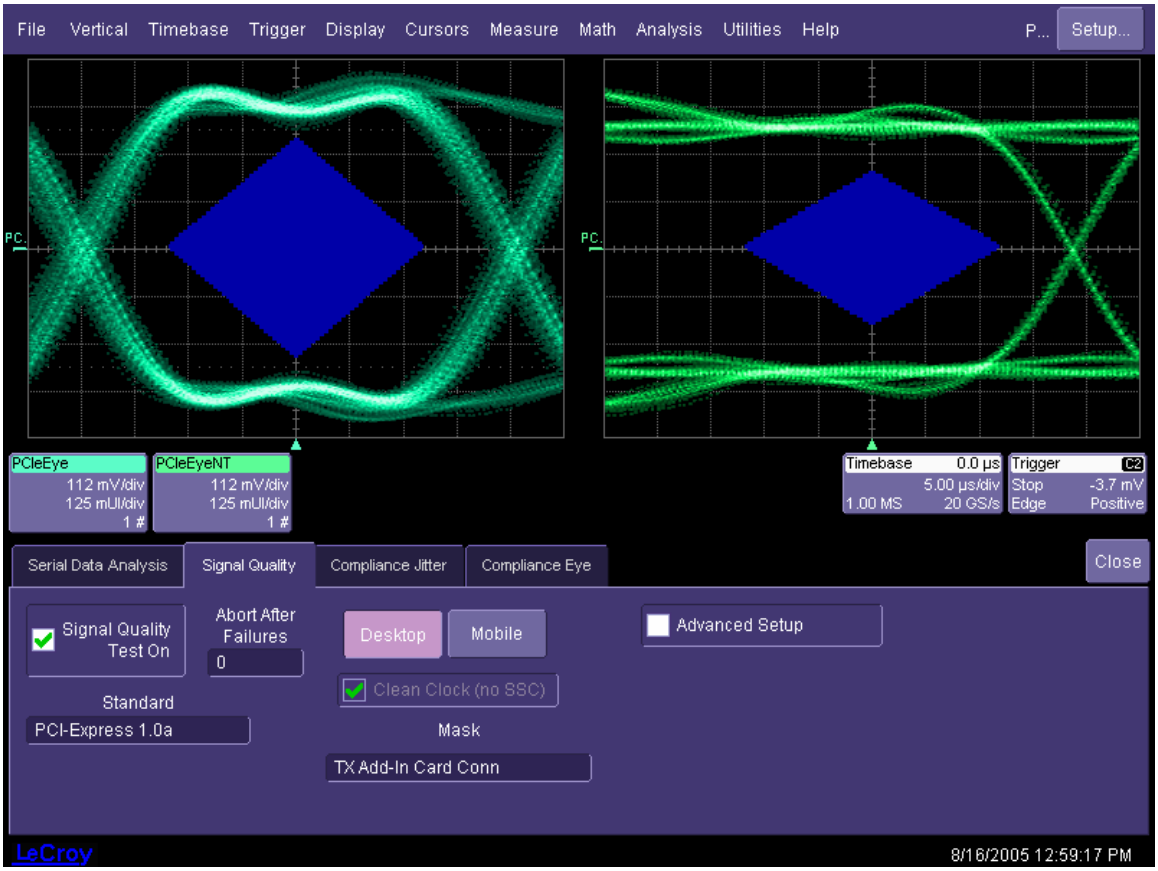


Figure 12. Add-In Card Test

The **Standard** control allows you to select PCI-Express v1.0a, PCI-Express v1.1, or PCI Express v2.0 (SDA 11000 only) as the signal under test. The **Abort After Failures** control will terminate the acquisition after the number of mask violations specified in this field. Whenever **Add-In card Masks** are selected, the **Clean Clock** checkbox is checked by default. For Tx or Rx package pin tests, however, selection of a clean clock is optional. Finally, for System Board tests the clean reference clock is not permitted. The PCI Express application running under X-Replay contains extensive reference clock test routines to characterize the existence of a clean clock.

The **Advanced Setup** checkbox allows the individual adjustment of jitter and clock recovery window settings used in the creation of eye diagrams. These are different depending on the revision level of the PCI Express specification selected. For example, for PCI Express v1.1 add-in card, the following values are used:

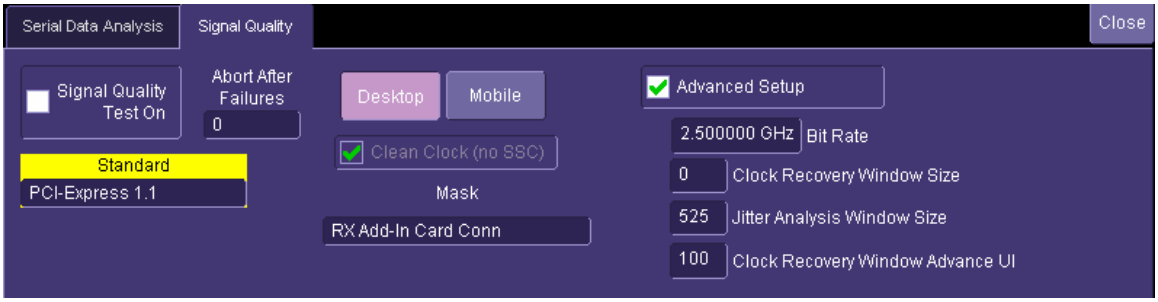
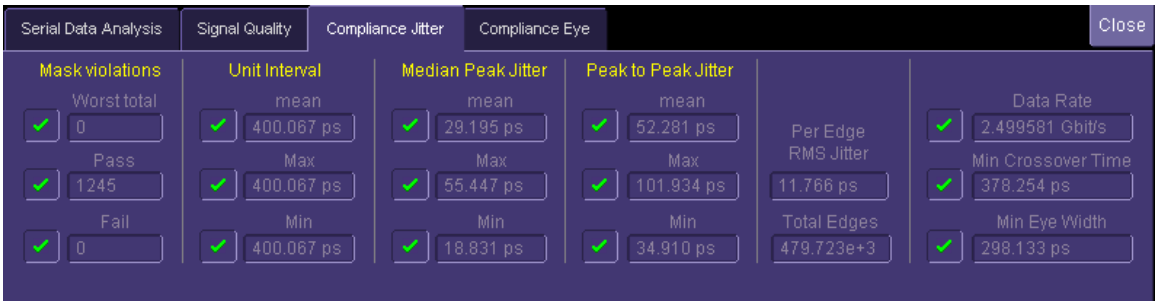


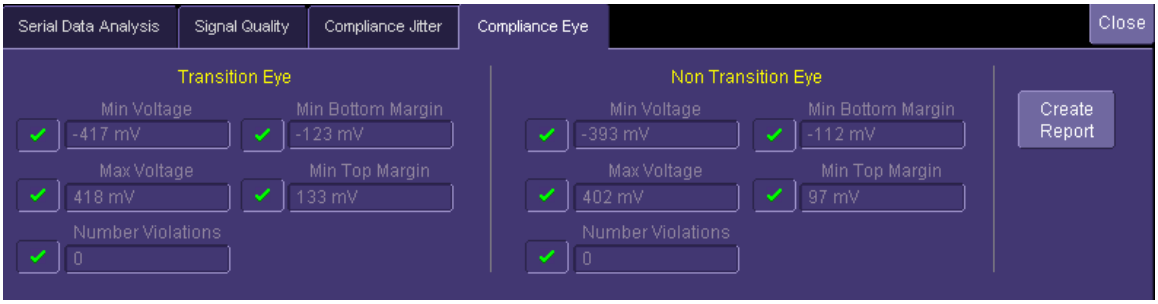
Figure 13. PCI Express Add-In Card Mask Settings (Tested with a Clean Clock)

The "**Compliance Jitter**" and "**Compliance Eye**" tabs display tables of jitter, timing, and voltage measurements. Each measurement has a checkbox to its left indicating pass or fail. A green check in this box indicates that the

corresponding parameter meets the compliance specification. A failure is indicated by a blank box adjacent to the parameter.



For the **Compliance Eye**:



The eye patterns and test results can also be exported to HTML using the **Create Report** button.

It is important to note that Compliance Testing, as defined by PCI-SIG, is a small subset of the electrical checklist considerations document. The X-Replay script (and report) covers many more tests.

Parameter List – Transmitter Compliance Tests (measured at the Tx package pins)

Test	Assertion	Parameter
Test 1.5	PHY.3.2#1	MaskViolationsTXNonTransition
Test 1.5	PHY.3.2#1	VtxMaxNonTransition
Test 1.5	PHY.3.2#1	VtxMinNonTransition
Test 1.5	PHY.3.2#14	VtxMobileMax
Test 1.5	PHY.3.2#14	VtxMobileMax
Test 1.5	PHY.3.2#14	VtxMobileMin
Test 1.5	PHY.3.2#14	VtxMobileMin
Test 1.5	PHY.3.2#14	MaskViolationsTXMobile
Test 1.5	PHY.3.2#14	MaskViolationsTXMobile
Test 1.5	PHY.3.2#14	MaskViolationsTXMobile
Test 1.5	PHY.3.2#2	Vtx-diffp-p
Test 1.5	PHY.3.2#2	VtxMaxTransition
Test 1.5	PHY.3.2#2	VtxMinTransition
Test 1.5	PHY.3.2#2	MaskViolationsTXTransition
Test 1.5	PHY.3.3#1	MaskViolationsTXTotal
Test 1.5	PHY.3.3#2	MaxUI

Test 1.5	PHY.3.3#2	AvgUI
Test 1.5	PHY.3.3#2	MinUI
Test 1.5	PHY.3.3#4	TtxEyeMedianToMaxJitter
Test 1.4	PHY.3.3#4	TtxEyeMedianToMaxJitter
Test 1.4	PHY.3.3#4	TtxEyeMedianToMaxJitter
Test 1.4	PHY.3.3#9	TtxEye

Parameter List – Add-In Card Compliance Tests (measured at the connector)

Test	Assertion	Parameter
Test 1.5	EM.4#19	VtxaMax
Test 1.5	EM.4#19	MaskViolationsAddInNonTransition
Test 1.5	EM.4#19	Vtxa_dMin
Test 1.5	EM.4#19	VtxaMin
Test 1.5	EM.4#19	Vtxa_dMax
Test 1.5	EM.4#19	MaskViolationsAddInTransition
Test 1.5	EM.4#19	JtxaMedianToMaxJitter
Test 1.5	EM.4#19	Ttxa

Parameter List – System Board Compliance Tests (measured at the connector)

Test	Assertion	Parameter
Test 1.5	EM.4#20	VtxsMax
Test 1.5	EM.4#20	VtxsMin
Test 1.5	EM.4#20	MaskViolationsSysTransition
Test 1.5	EM.4#20	Ttxs
Test 1.5	EM.4#20	JtxsMedianToMaxJitter
Test 1.5	EM.4#20	Vtxs_dMax
Test 1.5	EM.4#20	Vtxs_dMin
Test 1.5	EM.4#20	MaskViolationsSysNonTransition

Performing a PCI Express Simple Measurement

A second button is provided in the interface that accesses a set of additional measurements that are part of the PCI Express Base specification but not strictly required in Compliance mode. These measurements are selected by clicking or touching the **PCIe Measurement** button in the SDA main menu. The PCI Express Measurement mode contains a dialog with a measurement selection control. Some measurements such as common mode voltage require separate connections for the D^+ and D^- signals; two controls for the input sources are provided for these measurements. Measurements are performed by selecting the input sources and selecting the desired measurement from the control.

Note: Only measurements that require separate connections for the D^+ and D^- signals use the channels selected in the PCIe measurements menu. All other measurements use the waveform selected in the “Data Source" control in the SDA main menu.

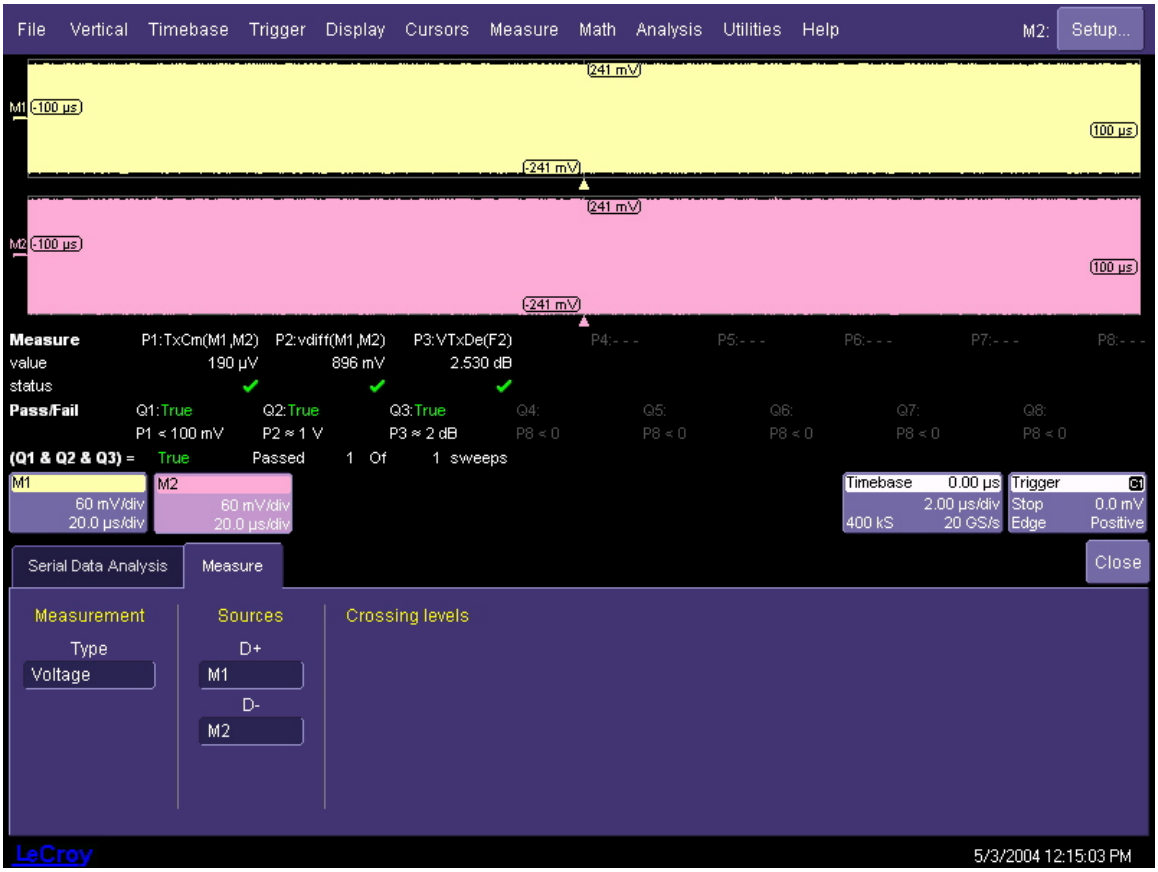


Figure 14. PCI Express voltage measurements. Note the measurements displayed in parameters P1 and P2 use the signals in sources D^+ and D^- (M1 and M2 in this case). The de-emphasis measurement (P3) uses the difference waveform between the D^+ and D^- (defined here in math function F2) and selected in the "Data Source" control in the SDA menu.

Voltage measurements

1. Select the input sources for the measurements. Enter the channels connected to the D^+ and D^- signals in the appropriate controls.
2. Select **Voltage** in the "Measurement" control.
3. The voltage measurements will appear below the grid area on the instrument as follows:

Note: The value of the differential peak-to-peak output voltage (P2) is tested against the required value at the transmitter device package pins. The measured value at the CBB or CLB will be lower and could indicate a failure in Q2. The compliance requirements are set by the eye patterns.

Parameter Number	Measurement	Explanation
P1	Transmitter DC common mode voltage	The average value of the waveform formed by adding the D^+ and D^- signals (V_{CMDC} = mean((D^+ + D^-)/2))
P2	Differential peak to peak output voltage	Measured as the p-p value of 2*| D^+ - D^-|
P3	Transmitter de-emphasis ratio	The log of the ratio of the p-p voltage for a transition bit to the p-p voltage of a non-transition bit computed as $20*\log_{10}(V_t/V_{nt})$

Timing measurements

1. Select the input sources for the measurements. Enter the channels connected to the D^+ and D^- signals in the appropriate controls.
2. Select **Timing** in the "Measurement" control.
3. The timing measurements will appear below the grid area on the instrument as follows:

Note: The value of the differential peak-to-peak output voltage (P2) is tested against the required value at the transmitter device package pins. The measured value at the CBB or CLB will be lower and could indicate a failure in Q2. The compliance requirements are set by the eye patterns.

Parameter Number	Measurement	Explanation
P1	Tx Rise Time D^+	Transition time, from 20% to 80% for all rising edges in the acquisition, as a fraction of a UI (1 UI= 400 ps for Gen 1)
P2	Tx Fall Time D^+	Transition time, from 80% to 20% for all falling edges in the acquisition, as a fraction of a UI (1 UI= 400 ps for Gen 1)
P3	Tx Rise Time D^-	Transition time, from 20% to 80% for all rising edges in the acquisition, as a fraction of a UI (1 UI= 400 ps for Gen 1)
P4	Tx Fall Time D^-	Transition time, from 80% to 20% for all falling edges in the acquisition, as a fraction of a UI (1 UI= 400 ps for Gen 1)

SSC measurements

1. Select the input sources for the measurements. Enter the channels connected to the source and destination signals in the appropriate controls. They are two directions on same lane. Signals can be input using several probing arrangements:
    a) two single ended probes - seeing half of each signal, or
    b) two diff probes (for SDA 6000A, these probes should be in channels 2 and 3),
    c) 4 single-ended SMA probes - the sources are two math functions that subtract the input pairs (SDA 6020)
2. Select "SSC" in the [Measurement] control.
3. The SSC measurements will appear below the grid area on the instrument as follows:

Parameter Number	Measurement	Explanation
P1	SSC Min	Ratio of minimum to max transfer rate. Pass if > 2.49G UI
P2	SSC Max	Ratio of minimum to max transfer rate. Pass if < 2.5G UI
P3	SSC Frequency Signal 1	Frequency of SSC Track, must be between 30 and 33 kHz
P4	SSC Min	Ratio of minimum to max transfer rate. Pass if > 2.49G UI
P5	SSC Max	Ratio of minimum to max transfer rate. Pass if < 2.5G UI
P6	SSC Frequency Signal 2	Frequency of SSC Track, must be between 30 and 33 kHz

CHECKLIST TEST MODE OF OPERATION

All the tests covered by this Manual refer to the PHY Electrical Test Considerations Rev 1.0, dated April 26, 2004. This section covers use of X-Replay and the supplied “Phy Tests Checklist.irt” script to perform tests described in the PHY Electrical Test Considerations, and to generate a report from X-Replay using the supplied stylesheet “XReplayPCIE_Report.xslt”

X-Replay allows you how to test PCI Express functionality in several ways:

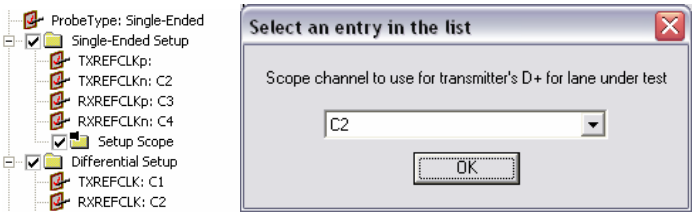
- Select, repeat, and skip tests as required to demonstrate or develop different PHY functions.
- Establish Test Limits for each of the versions of the PCI Express specification, and modify create or delete entire test limit sets.
- Generate Test Reports based on the tests actually run.
- Query the database for test results from prior test sessions or experiment runs.

The X-Replay application display is divided into several windows (clockwise, from upper left hand):

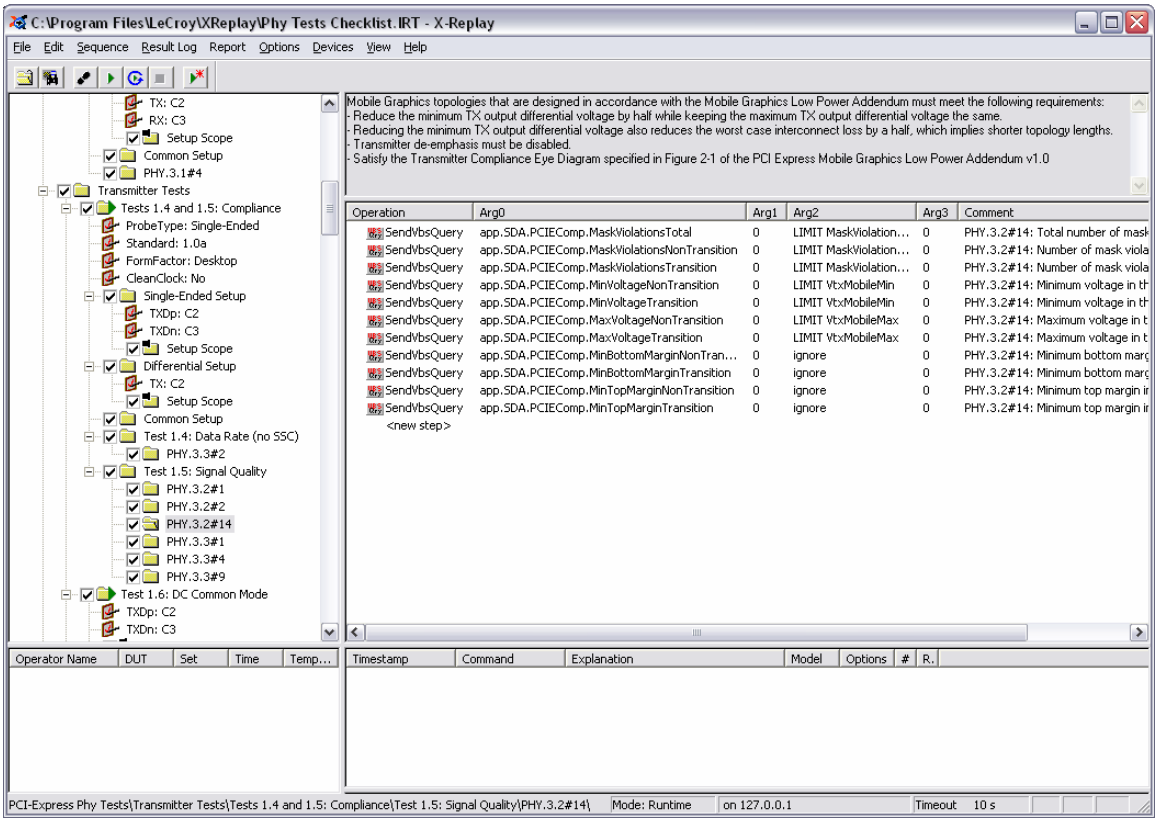
- Test Sequence Window
- Test Description Window
- Commands Window
- Activity Log Window
- Session Window

Use of Configuration Variables in Test Sequences

Configuration Variables allow you to define system inputs such as signal sources, probe types, specification parameter set to be used for testing, form factors, and other global conditions. These variables can be set prior to the start of testing, or changed in between test runs.



Right-clicking on any variable allows you to reset the variable to its default setting or to change the value to be used for subsequent tests.

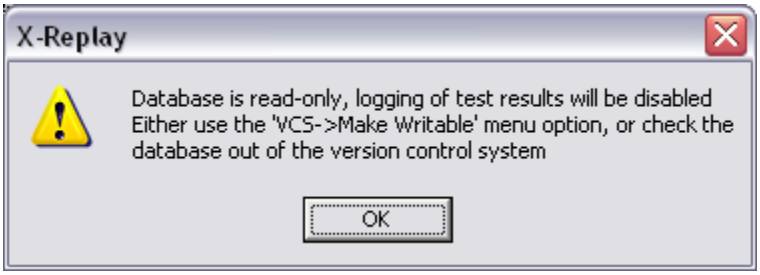


Menu Structure

File

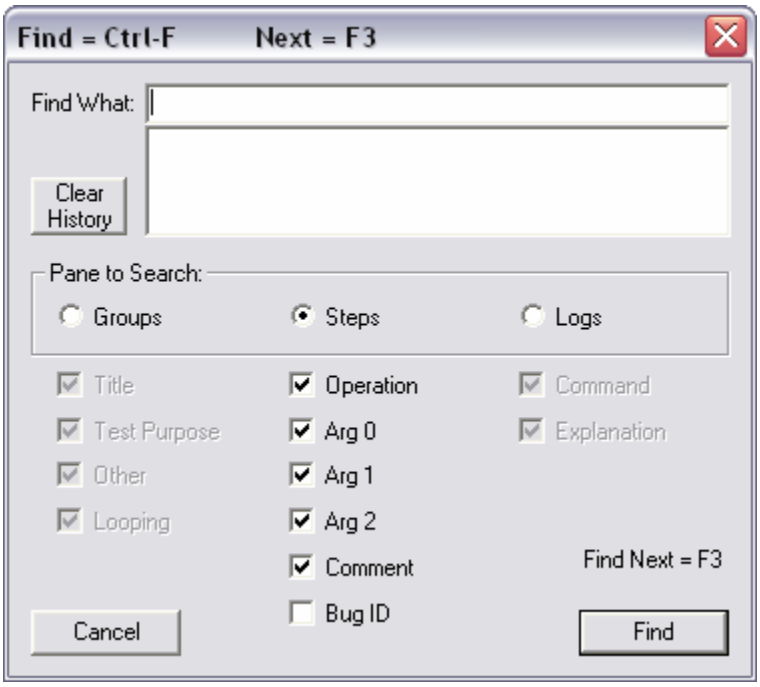
Open Test File (Test Database). The file extension is *.irt

Make Read Only disables the writing of test results to a session log. *Make Writable* reverses the action.



Edit

Performs the find function to locate specific measurements or actions in the program sequence.

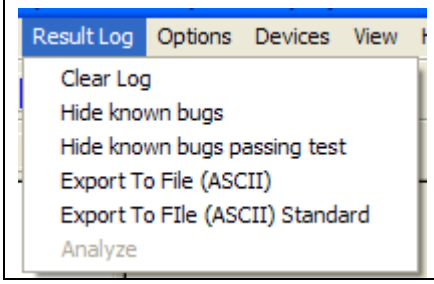


Sequence

Execute program items starting at the designated point. The menu bar displays the available choices:

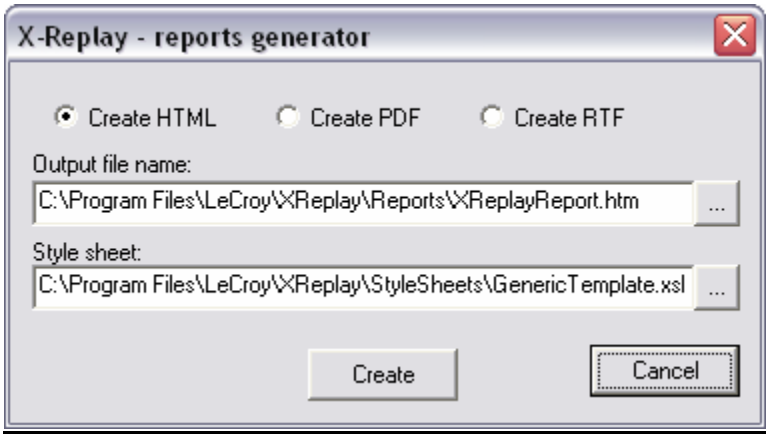
	*Open*
	*Searches Attached Devices* – performs a scope search
	*Single Step [F10]* – executes one instruction at a time
	*Play Selected Group and Children [F5]* – executes all the checked items in the selected group
	*Play selected group Continuously* – executes all checked items in the selected group until *Stop*
	*Stop* stops execution – (active when Play has been pressed)

Result Log

	*Clear Log* – removes all the previously recorded activity
	Export to File (ASCII) – creates a comma-separated-values set of activity records
	Export to File (ASCII) Standard – creates a text file phy tests checklist.logdump.txt

Report

Creates a report with one of three formats (html, pdf or rtf) based on the specified report template Style Sheet (*.xsl or *.xslt). For Style Sheet, select the supplied “XReplayPCIE_Report.xslt”. The **…** button to the right of the text entry field can be used to browse and find that file. On an SDA, it should be found in D:\Applications\PCIE.



Options

Select the Limits option to allow the configuration of individual parameters pass/fail criteria, or edit, rename and save complete parameter sets.

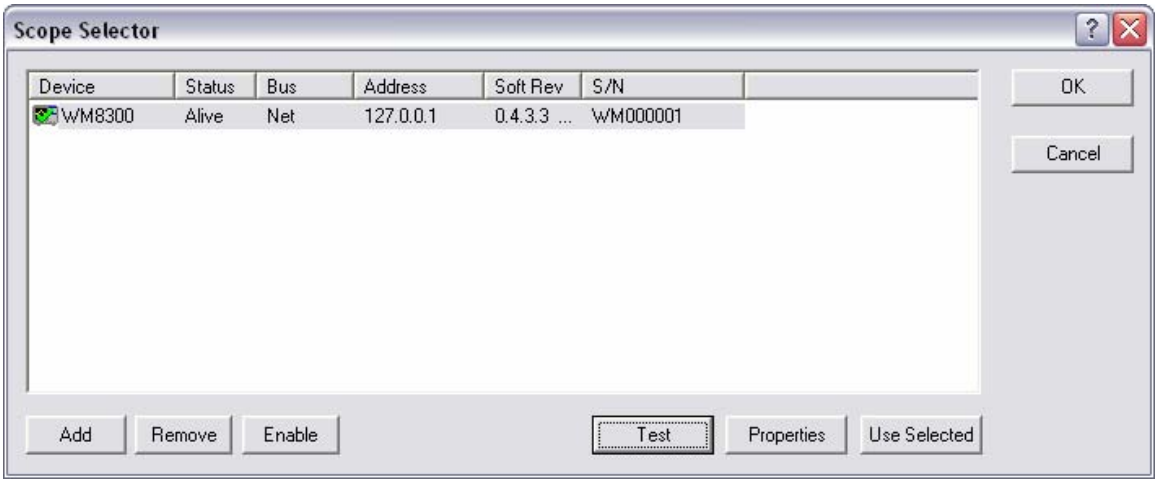
Create Set – You can create a new, named set of limits . Initially, the new set is the same as the set selected when you press **Create Set**.

Edit Limit – Using Edit Limit allows limits to be changed to meet specific pass/fail criteria.

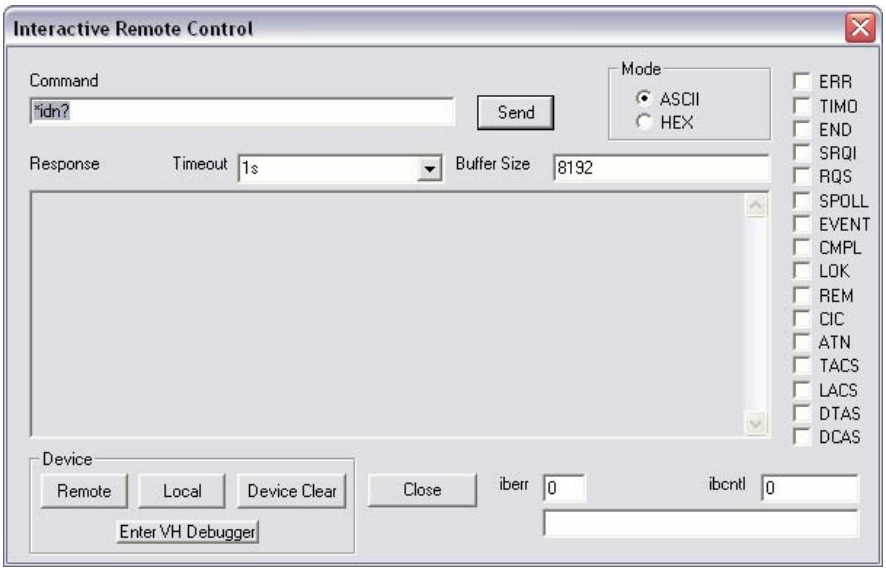
Import/Export Limits – Allows you to transfer entire parameter sets to csv-formatted (MS Excel) files.

Devices

Scope Manager – Displays the devices connected to the host computer. There are two supported modes of attaching a device: GPIB or LAN.



Interactive Dialog – Supports sending and receiving single line commands to the device(s) on the list.



View

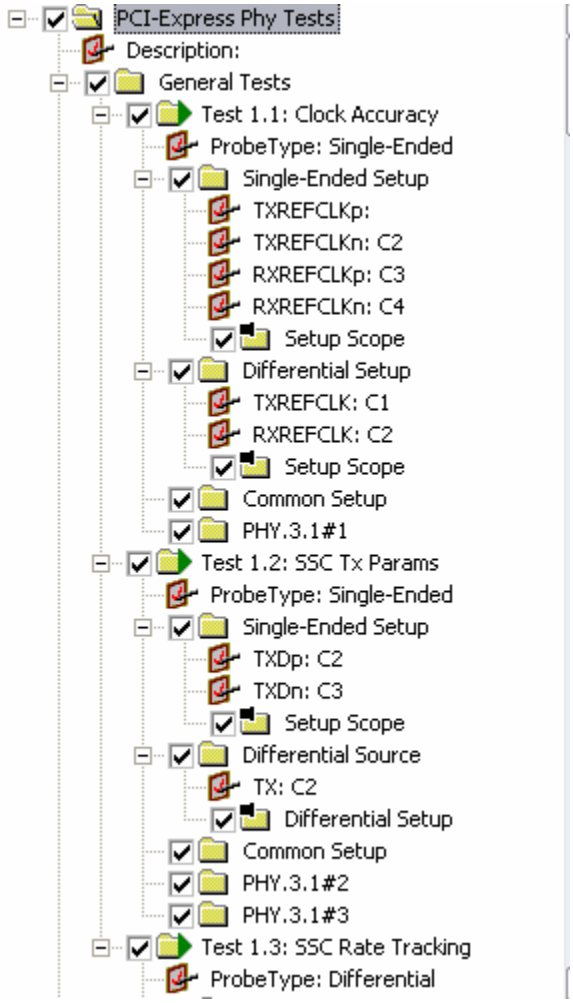
Enables/Disables Toolbar and Status bars

Help

Help Topics

Running PCI Express Tests

1. Verify proper signal input and observe all deskew and calibration procedures.
2. Run X-Replay application.
3. Open the PHY Tests Checklist database.
4. Select the test(s) group(s) to be executed.
5. Set up ***Configuration Variables*** as required for the selected tests.
6. Press **Play** and follow script prompt(s) as required



Export to *.XML file – Database Access

X-Replay allows you to export the entire test session(s) to XML file for subsequent access by database programs such as Microsoft Access. Most database programs have built-in XML import data capability. Please note that test sessions appear at the lower left portion of the X-Replay window.

In order to create an XML record of the session data, right-click the desired test session and select **Dump Log into XML**.

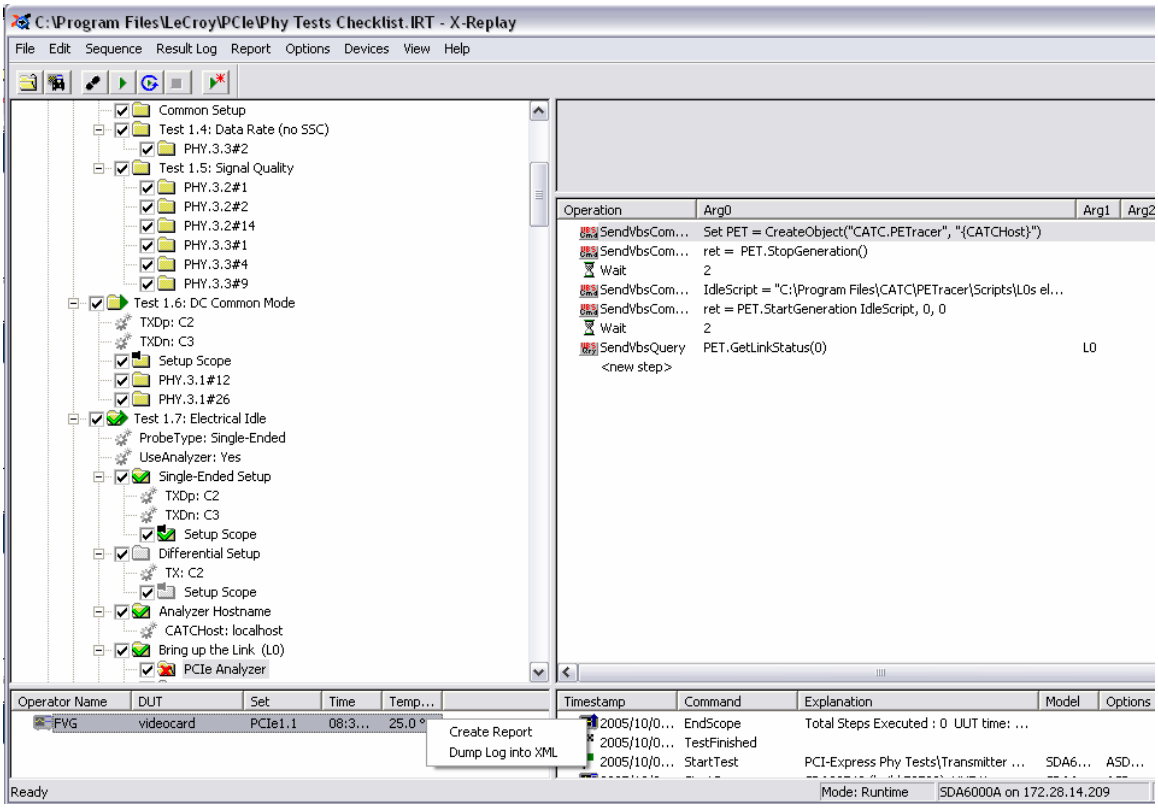


Figure 15. Saving test results to *xml format

TEST SEQUENCE REFERENCE

General Information (Batch/Device Info)

Purpose: Space provided in X-Replay window to enter Device-specific Information (alphanumeric)

Available Entries:

Enter first Lane-ID

Enter second LaneID

PCI Express Tests

GENERAL TESTS

Clock Accuracy - Test 1.1

Assertion: PHY.3.1#1

Purpose: Test Bit Rate Clock Accuracy

Description:

1. Measure the bit rate clock source for the transmitter, using a frequency counter or equivalent. If spread spectrum (SSC) is used, a modulation domain analyzer is recommended for complete spread spectrum characterization of the 100 MHz reference clock.
2. Measure the bit rate clock source for the receiver using a frequency counter or equivalent. If SSC is used, a modulation domain analyzer is recommended for complete spread spectrum characterization of the 100 MHz reference clock.

3. Verify that the bit rate clocks for the transmitter and receiver of each link are within 600 ppm of each other at all times in both SSC and non-SSC modes. One possible method is to use a real-time oscilloscope to capture outputs from both clocks simultaneously and use post-processing software to calculate and compare the frequency of each clock at any given time in the sample.

SSC Tx Params: Test 1.2

Assertions: PHY.3.1#2, PHY.3.1#3

Purpose: Test SSC Transmitter Data and Modulation Rate

Method:

1. Place transmitter under test in compliance pattern mode.
2. Measure transmitted waveform with high-speed oscilloscope. To accurately test the minimum SSC modulation rate, the measurement should be performed for at least 30.3 µs.
3. Compute data rate from waveform data. Compute SSC modulation rate from waveform data.

SSC Rate Tracking: Test 1.3

Assertion: PHY.3.1#4

Purpose: Test SSC Transmitter Data Rate Tracking

1. Place one end of a PCI Express Link in loopback mode.
2. During data transfer, measure the transmitter data rates on the upstream and corresponding downstream paths simultaneously.
3. Verify that the two communicating ports do not exceed 600 ppm.

Note: This test can be performed during normal data transfers.

TRANSMITTER TESTS

Tests 1.4 and 1.5: Compliance

Assertions: PHY.3.3#2, PHY.3.2#1, PHY.3.2#2, PHY.3.2#14, PHY.3.3#1, PHY.3.3#4, PHY.3.3#9

Purpose: Non-SSC Transmitter Data Rate (Test 1.4)

The PCI-Express Base Specification, Rev 1.1 requires that jitter measurements be met with a sample size of 1 million UI. This test uses a 50 µs (125k UI) acquisition; therefore, for compliance this test should be run 8 times.

1. Attach the Compliance Test Load on all the transmitter data lines for the DUT.
2. Place the transmitter in compliance pattern mode.
3. Measure the transmitted waveform with a high-speed oscilloscope.
4. Generate an eye pattern diagram from the data.
5. Compare with PCI Express transmit eye pattern specified for the probing location.
6. Compute the time between the jitter median and the maximum deviation from the median.

Note: Mobile Graphics that are designed in accordance with the Mobile Graphics Low Power Addendum must have de-emphasis disabled.

Test 1.6: DC Common Mode

Assertions: PHY.3.1#12, PHY.3.1#26

Purpose: Measure TX DC Common Mode Voltage

Method:

1. Using the math functions of an oscilloscope or using post processing software, measure the TX DC common mode voltage for all states.
2. Measure the absolute delta of DC common mode voltage between D^+ and D^-.

Note: $V_{CM} = [VD^+ + VD^-]/2$ (As defined in the PCI-Express Base Specification, Sec. 4.3.2)

Note: Getting a device to transition from L0 to Electrical Idle requires the use of Protocol-Specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. For tests that require the device to remain in electrical idle, the L1 Power Management script is used. See Appendix A for an example of this setup.

Test 1.7: Electrical Idle

Assertions: PHY.3.1#23, PHY.3.1#24, PHY.3.1#27

Purpose: Tx Transition from L0 to Electrical Idle to L0

Method:

1. Set up the oscilloscope to trigger when the transmitter transitions to electrical idle.
2. Force the DUT transmitter to issue the Electrical Idle ordered-set and transition to Electrical Idle.
3. Verify that the DUT sends a K28.5 (COM) followed by three K28.3 (IDL) before entering Electrical Idle.
4. Verify the transmitter is in a valid Electrical Idle state within 20 UI of the last symbol of the Electrical Idle ordered-set.
5. Rerun the above steps while forcing the DUT to transition from L0 to Electrical Idle to L0 again using implementation-specific hardware or software methods.
6. Verify the transmitter remains in Electrical Idle for a minimum of 50 UI.

Note: Getting a device to transition from L0 to Electrical Idle and back to L0 requires the use of protocol-specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. For tests that require the device to return to L0, the L0 Electrical Idle script is used. See Appendix A for an example of this setup.

Test 1.8: RX Detect Voltage

Assertion: PHY.3.1#14

Purpose: RX Detect - Maximum Voltage Change

Method: Measure the maximum change in voltage during receiver detection.

Note: Getting a device to transition from L0 to Electrical Idle requires the use of protocol-specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. See Appendix A for an example of this setup.

Test 1.9: RX Detect Hi-Z

Assertion: PHY.3.1#17

Purpose: RX Detection - High Receiver Impedance

Method:

1. Place 200 kohms (Zrx-com-high-imp-dc Min) to ground in parallel with 3 nF on the transmitter data lines.
2. Verify that the associated TXs of the DUT do not enter CMM.

Test 1.10: RX Detect Low-Z

Assertion: PHY.3.1#18

Purpose: RX Detection - Low Receiver Impedance

Method:

1. Place 40 ohms (Zrx-com-dc Min) in series with 75 nF (Ctx Min) to ground on the transmitter data lines.

2. Verify that the associated TXs of the DUT enter CMM.

Test 1.11: Lane Skew

Assertion: PHY.3.3#8

Purpose: Lane-to-Lane Output Skew

Method:

1. Place all lanes of the device under test in compliance pattern mode.
2. Measure the bit-to-bit skew between all Lanes of the same Link. Ensure the measurement is made on equivalent data state transitions.

Test 1.12: Rise/Fall

Assertion: PHY.3.3#3

Purpose: TX Output Rise/Fall Time

Method:

1. Connect 50 ohm loads to ground to the package pins of the silicon under test.
2. Place the silicon under test in polling compliance mode.
3. Measure the timing and voltage parameters within 0.2 inches of the package pins.

Note: For more accurate results this measurement should be made using an SDA 11000.

Test 1.15: Idle Voltage

Assertion: PHY.3.3#6

Purpose: TX Electrical Idle Voltage

Method:

1. Set up the oscilloscope to trigger when the transmitter transitions to electrical idle.
2. Force the DUT transmitter to issue the Electrical Idle ordered set and transition to Electrical Idle.
3. Verify that the DUT sends a K28.5 (COM) followed by three K28.3 (IDL) before entering Electrical Idle.
4. Verify that the transmitter is in a valid Electrical Idle state within 20 UI of the last symbol of the Electrical Idle ordered-set.
5. Verify that the Electrical Idle differential peak output voltage is no greater than 20 mV.

Note: For a symmetric differential swing, $V_{DIFFp} = \max(|V_{D+} - V_{D-}|)$ as defined in the PCI-Express Base Specification, Sec. 4.3.2

Note: Getting a device to transition from L0 to Electrical Idle requires the use of protocol-specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. For tests that require the device to remain in electrical idle, the L Power Management script is used. See Appendix A for an example of this setup.

Test 1.16: Idle Transition

Assertion: PHY.3.1#19

Purpose: TX Transitions from Electrical Idle

Method:

1. Set up the oscilloscope to trigger when the transmitter transitions from electrical idle to sending differential data.
2. Force the DUT transmitter to leave Electrical Idle.
3. Verify that the DUT meets all TX differential signal specifications within 20 UI.

Note: Getting a device to transition from L0 to Electrical Idle requires the use of protocol-specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. For tests that require the device to remain in electrical idle, the L1 Power Management script is used. See Appendix A for an example of this setup.

Note: Mobile Graphics that are designed in accordance with the Mobile Graphics Low Power Addendum must meet the transmitter eye requirements of the addendum.

Test 1.17: RX Detect Sequence

Assertions: PHY.3.1#30, PHY.3.1#31, PHY.3.1#32, PHY.3.1#33

Purpose: Receiver Detection Sequence

Method:

1. Set up the oscilloscope to trigger on the Receiver Detection sequence.
2. Verify that the transmitter starts at a stable voltage between VDD and GND prior to performing the common-mode shift.
3. If the common-mode voltage is equal to VDD, the shift must be towards GND.
4. If the common-mode voltage is equal to GND the shift must be towards VDD.
5. If the common-mode voltage is between VDD and GND the shift must be in the opposite direction the voltage moved to get to this initial common-mode voltage.

Test 1.18: Beacon or Wake#

IMPORTANT NOTE: This Test is not supported.

Test 1.19: Electrical Idle Exit

Assertion: PHY.3.3#7

Purpose: Electrical Idle Exit Detection

Method:

1. Place the DUT into Electrical Idle.
2. Set up the oscilloscope to trigger when the transmitter leaves electrical idle.
3. Using a data generator or other type of signal source, verify that the DUT exits Electrical Idle when a signal larger than 65 mV_{diffpp} is detected at the DUT receiver.
4. Using a data generator or other type of signal source verify that the DUT does not exit Electrical Idle when a signal less than or equal to 65 mV_{diffpp} is present at the DUT receiver.

Note: Getting a device to transition from L0 to Electrical Idle requires the use of protocol-specific tools. LeCroy implements its protocol level using the PE Tracer/Trainer Exerciser and Analyzer. For tests that require the device to remain in electrical idle the L1 Power Management script is used. See Appendix A for an example of this setup.

Test 1.29: Beacon Propagation

IMPORTANT NOTE: This Test is not supported.

Test 1.30: Wakeup Propagation

IMPORTANT NOTE: This Test is not supported.

Receiver Tests

Test 1.14: DC Common Mode

Assertion: PHY.3.1#11

Purpose: RX DC Common Mode Voltage

Method:

1. Using a DVM, measure the DC voltage with respect to ground of RX D^+ (PERpX) and D^- (PERnX) for all lanes. Ensure the ground referenced is near the component silicon ground.

Note: This test requires additional hardware (not supplied).

Test 1.20: DC Impedance

Assertion: PHY.3.1#10

Purpose: Receiver DC Differential Mode Impedance

Method:

1. Connect the DUT to the Compliance Test Load.
2. Apply power to the DUT.
3. Measure the DC differential mode impedance of each RX using a DVM.

Test 1.21: Receiver Sensitivity

IMPORTANT NOTE: This Test is not supported.

Test 1.22: Unexpected Idle

IMPORTANT NOTE: This Test is not supported.

Test 1.23: Skew

IMPORTANT NOTE: This Test is not supported.

SYSTEM BOARD TESTS

Test 1.5: Signal Quality (Compliance)

Assertions: EM.4#14, EM.4#16, EM.4#20

Purpose: Signal Quality

Method:

1. Attach the Compliance Test Load on all the transmitter data lines for the DUT.
2. Place the transmitter in the compliance pattern mode.
3. Measure the transmitted waveform with a high-speed oscilloscope.
4. Generate an eye pattern diagram from the data.
5. Compare with the PCI Express transmit eye pattern specified for the probing location.
6. Compute the time between the jitter median and the maximum deviation from the median.

Note: PCI-Express Card Electromechanical Specification, Rev 1.1, requires that the jitter measurements be met with a sample size of 10 million UI.

Test 1.21: Receiver Sensitivity

IMPORTANT NOTE: This Test is not supported.

Assertion: EM.4#22

Purpose: Receiver Sensitivity

Test 1.24: V_{AUX} Power (wake)

Assertion: EM.4#4

Purpose: Wake Enabled Platform V_{AUX} Power

Method:

1. Measure the +3.3 V_{AUX} voltage with no load attached for each PCI Express connector.

2. Attach a 375 mA resistive load to the +3.3 V_{AUX} rail for each PCI Express connector that is wakeup enabled.
3. Verify that the +3.3 V_{AUX} rail voltage meets specification requirements for each connector under loaded conditions.

Note: This test requires additional hardware (not supplied).

Test 1.25: V_{AUX} Power (non-wake)

Assertion: EM.4#5

Purpose: Non-Wake Enabled Platform V_{AUX} Power

Method:

1. Measure the +3.3 V_{AUX} voltage with no load attached for each PCI Express connector.
2. Attach a 20 mA resistive load to the +3.3 V_{AUX} rail for each PCI Express connector.
3. Verify that the +3.3 V_{AUX} rail voltage meets specification requirements under fully loaded conditions.

Note: This test requires additional hardware (not supplied).

Test 1.26: Platform Power

Assertion: EM.4#7

Purpose: Platform Power

Method:

1. Measure the voltage of all the power rails with no load attached for each PCI Express connector.
2. Fully load each power rail for all PCI Express connectors.
3. Verify that the voltage rails voltage meets specification requirements under fully loaded conditions.

Note: This test requires additional hardware (not supplied).

Note: System boards designed in accordance with the 75W Power ECN must meet the additional power requirements.

Test 1.5: Signal Quality (Compliance)

Assertions: EM.4#13, EM.4#15, EM.4#19

Purpose: Signal Quality

Method:

1. Attach the Compliance Test Load on all of the transmitter data lines for the DUT.
2. Place the transmitter in compliance pattern mode.
3. Measure the transmitted waveform with a high-speed oscilloscope.
4. Generate an eye pattern diagram from the data.
5. Compare with the PCI Express transmit eye pattern specified for the probing location.
6. Compute the time between the jitter median and the maximum deviation from the median.

Note: PCI-Express Card Electromechanical Specification, Rev 1.1, requires the jitter measurements be met with a sample size of 10 million UI.

Test 1.21: Receiver Sensitivity

Assertion: EM.4#21

Purpose: Receiver Sensitivity

IMPORTANT NOTE: This Test is not supported

Test 1.27: Link Training

Assertion: EM.2#27

Purpose: Initial Active Link Training

Method:

1. Set up an oscilloscope to trigger on the end of PERST#.
2. Measure the time from the end of PERST# to the initial active Link Training state (exit electrical idle).

Note: Getting a device to exit Electrical Idle state requires the use of protocol-specific tools. LeCroy implements its protocol level exercises using the PE Tracer/Trainer Exerciser & Analyzer. See Appendix A for an example of this setup.

Test 1.28: Down-Shifting

Assertion: EM.6#4

Purpose: Down-Shifting x8 to x4

Method:

1. Connect the DUT to the x8 connector on the test platform. This x8 connector should have only the first 4 lanes routed.
2. Apply power to the platform.
3. Verify that the x8 add-in card is operating as a x4 card.

Test 1.31: Add-In Power

Assertion: EM.4#23

Purpose: Add-in Card Power

Method:

1. Plug the DUT into the compliance base board (CBB) which ideally terminates each transmitter lane.
2. Apply power to the CBB.
3. Measure the current drawn by the DUT for each power rail.

REFCLK Tests (PCIe1.1 only)

These tests refer to Table 2-1 "REFCLK DC Specifications and AC Timing Requirements" in section 2.1.3 of the PCI-Express Card Electromechanical Specification, Rev 1.1.

Changes from Version 1.0a

- Base Specification Changes:

  New clock recovery function for measuring eye diagrams

- CEM Specification Changes:

  Reference clock specification and sample sizes Base Board measurement with unfiltered reference clock

Single-Ended Tests

Input Voltage

Description:

REFCLK+ and REFCLK- must both be within the limits V_{MAX} and V_{MIN}, such that:

V_{MAX} = Absolute Max input voltage

= +1.15 V

V_{MIN} = Absolute Min input voltage

= -0.3 V

Where V_{MAX} is the maximum instantaneous voltage including overshoot, and V_{MIN} is defined as the minimum instantaneous voltage including undershoot. See Figure 2-4 of the PCI-Express CEM 1.1 Specification (reproduced below).

Crossing Voltage

Description: V_{CROSS} Absolute

Crossing point voltage +250 to +550 mV

Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

V_{CROSS} Absolute refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-4.

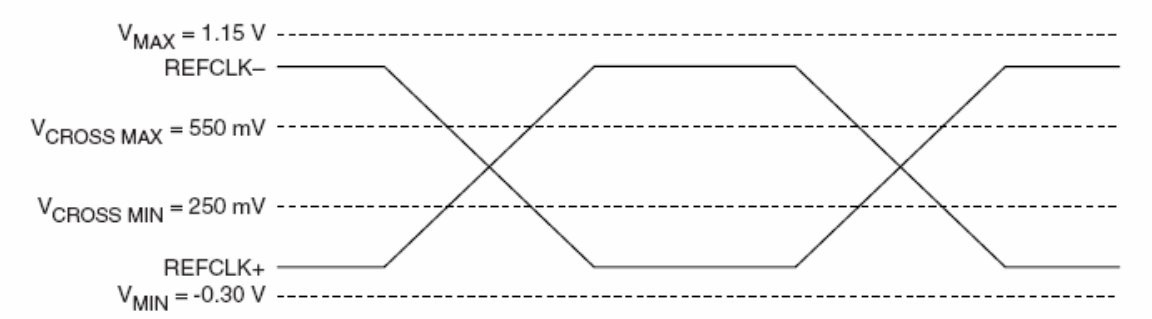


Figure 2-4. (from PCI Express CEM 1.1 specification)

$V_{CROSS\ DELTA}$ = Variation of V_{CROSS} over all rising clock edges +140 mV

Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 2-5.

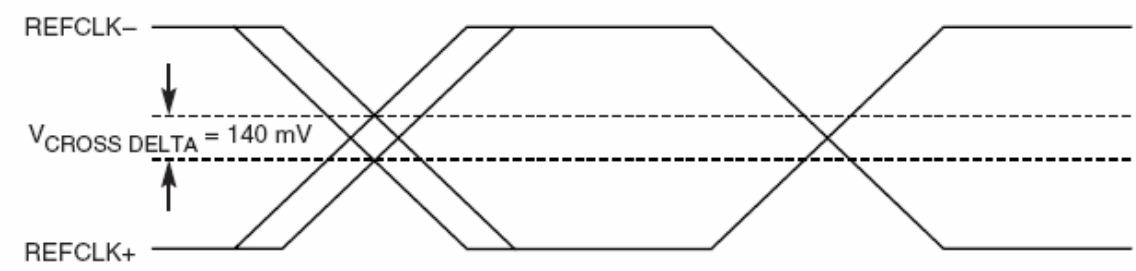


Figure 2-5. (from PCI Express CEM 1.1 specification)

Rise Fall Matching

Description: Rise-Fall Matching

Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching, max 20 %

Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 2-6 of the PCI-Express CEM 1.1 Specificiation.

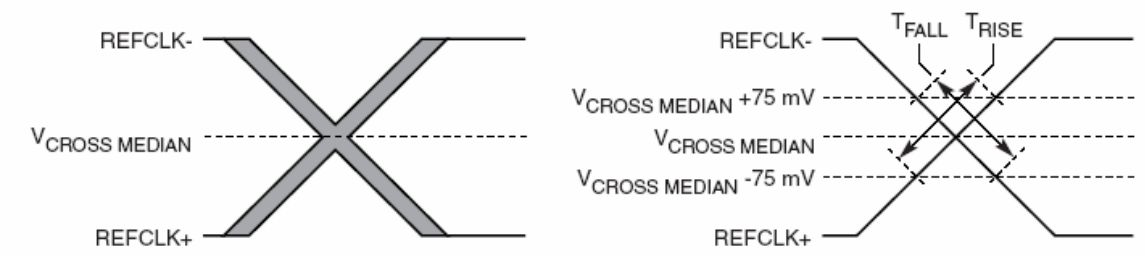


Figure 2-6. (from PCI Express CEM 1.1 specification)

Differential Tests

Edge Rate

Description: Rise Edge Rate

Limits:

min = 0.6 GV/s

max = 4.0 GV/s

Description: Fall Edge Rate

Limits:

min = 0.6 GV/s

max = 4.0 GV/s

Test Condition: Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 2-8 of the PCI-Express CEM Specification, Rev 1.1.

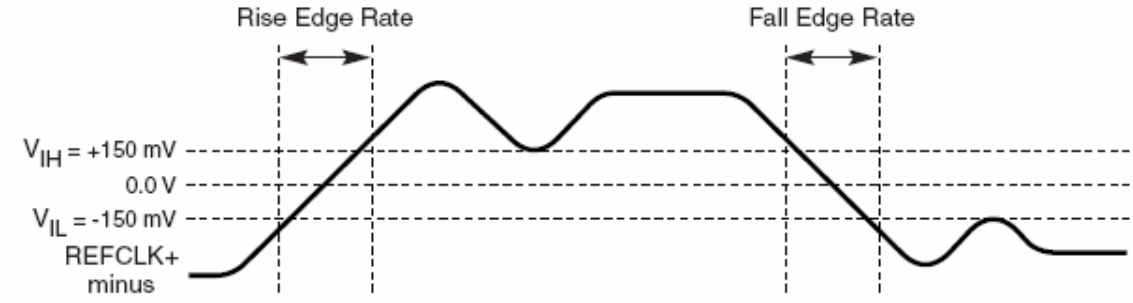


Figure 2-8. (from PCI Express CEM 1.1 specification)

Differential Voltage

Description:

V_{IH} = Differential Input High Voltage

min = +150 mV

V_{IL} = Differential Input Low Voltage

max = -150 mV

Ringback

Description:

V_{RB} = Ring-back Voltage Margin

min = -100,

max = +100 mV

T_{STABLE} = Time before V_{RB} is allowed

max = 500 ps

Note: T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the Vrb ±100 mV differential range. See Figure 2-9 of the PCI-Express CEM Specification, Rev 1.1.

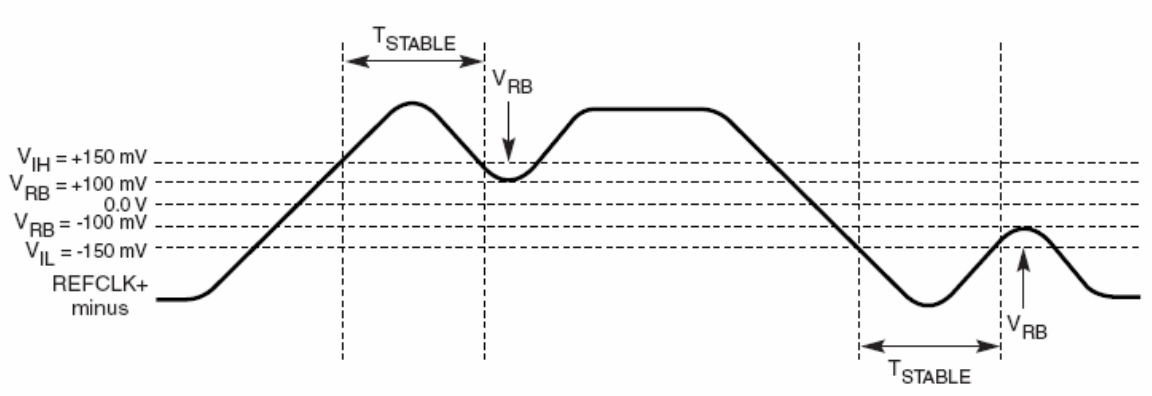


Figure 2-9. (from PCI Express CEM 1.1 specification)

Period

Description:

$T_{PERIOD\ AVG}$ = Average Clock Period Accuracy

Limits:

min= -300 ppm

max = +2800 ppm

Note: PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 ppm, then, we have an error budget of 100 Hz/ppm * 300 ppm = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 ppm applies to systems that do not use Spread Spectrum, or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 ppm nominal shift in maximum period resulting from the 0.5% down-spread, resulting in a maximum average period specification of +2800 ppm

$T_{PERIOD\ ABS}$ = Absolute Period (including Jitter and Spread Spectrum)

min = 9.847ns

max = 10.203 ns

Note: Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 2-7 of the PCI-Express CEM Specification, Rev 1.1.

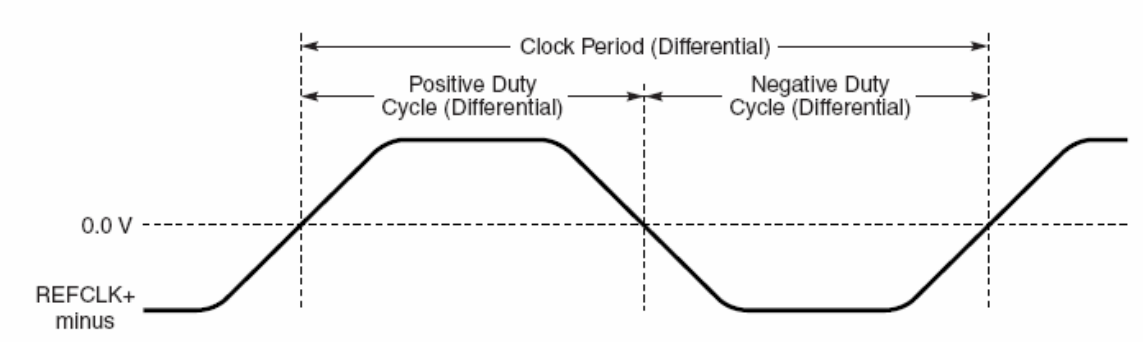


Figure 2-7. (from PCI Express CEM 1.1 specification)

Duty Cycle: min: 40%, max: 60%

- **SSC**

  Clock Period Accuracy min = -300 ppm, max = +2800 ppm

- **No SSC**

  Clock Period Accuracy min = -300 ppm, max = +300 ppm

§ § §

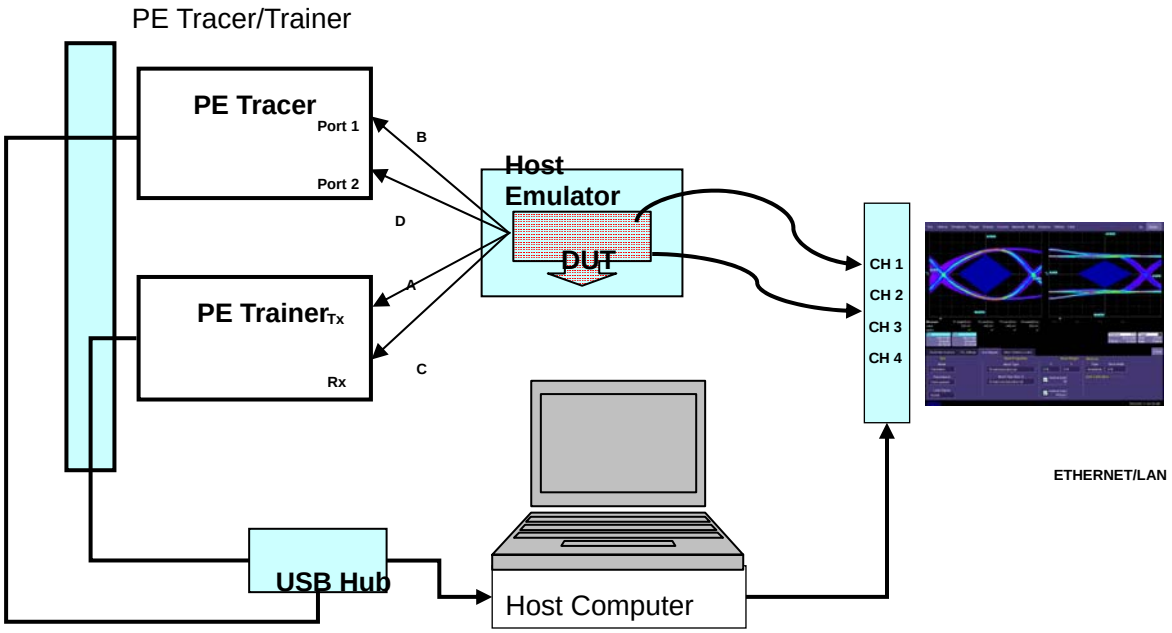
APPENDIX A – PROTOCOL ANALYZER AND PCI EXPRESS ELECTRICAL TESTS:

Use of Generation Files

LeCroy implements two generation files (files with extension *.peg in the PE Tracer/Trainer) to exercise the state of the DUT:

- L0s Electrical Idle peg , which forces the device under test to transition from L0 to Electrical Idle and back to L0 is used to implement Test 1.7
- L1 Power Management peg, which transitions the device under test to Electrical Idle, is used to implement Tests 1.6, 1.15, 1.16 and 1.19

Block Diagram –System Configuration

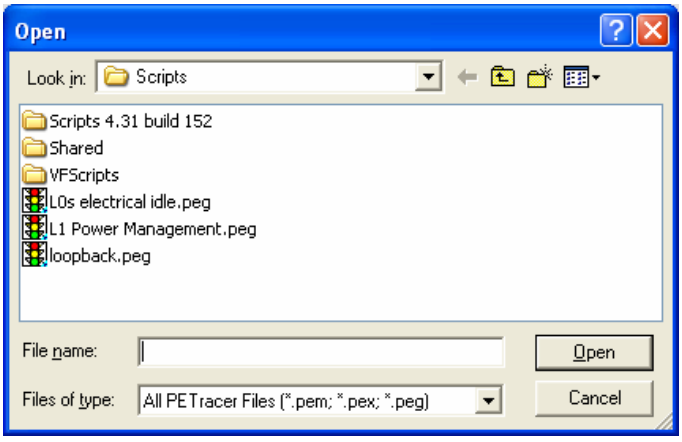


Step sequence for Test 1.7

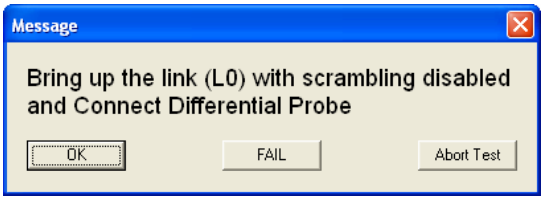
1. In the PE Tracer menu, Load Traffic Generation file (L0s Electrical idle.peg).
2. Bring up (Connect) link to initialize DUT in L0 state.
3. Transition DUT from L0 to Electrical Idle (resume generation) and back to L0.
4. Scope triggers in last K28.5,28.3,K28.3,K28.3 (trigger on pattern).
5. Test Passes if no exit from Electrical Idle for at least 50 UI (20 ns.).

Test Steps using X-Replay

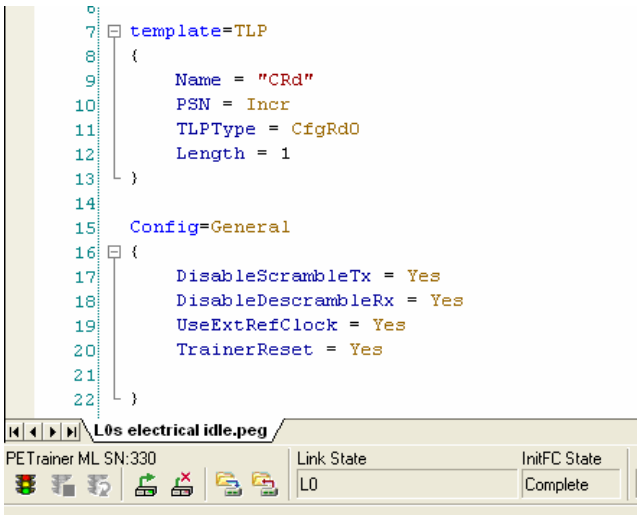
1. In the PE Tracer menu, Load Traffic Generation file L0s Electrical idle.peg:



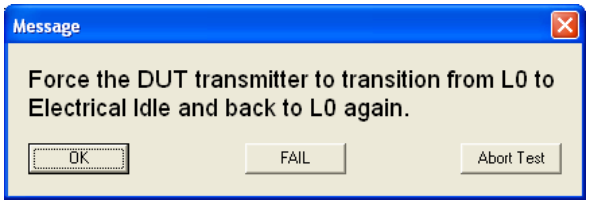
2. Bring up link to initialize DUT in L0 state.



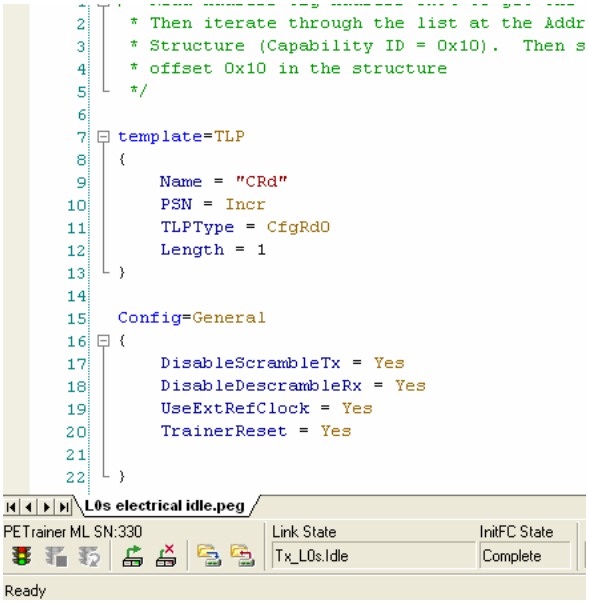
3. In The PE Tracer Menu, bring up the link. The screen should indicate Link State = L0.



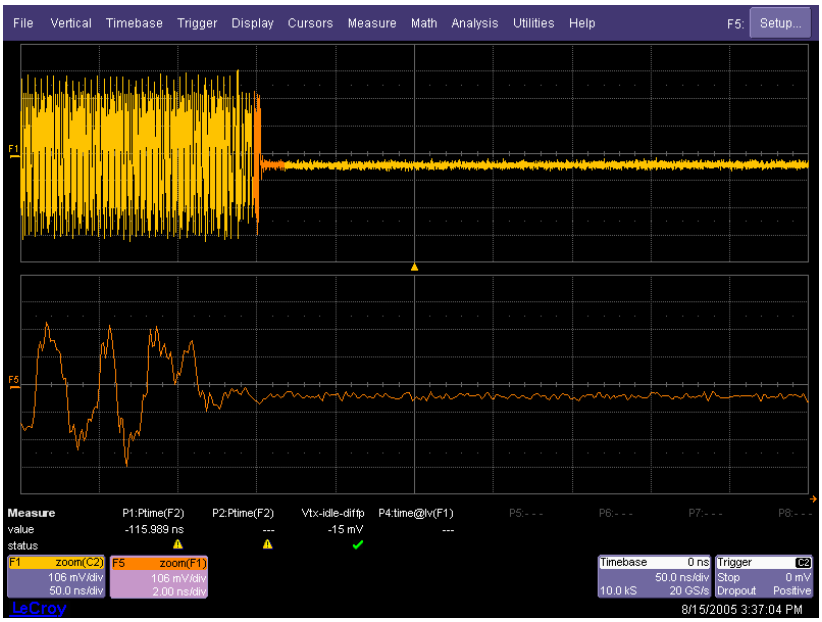
4. Start Generation. The Host emulator will transition the device from L0 to electrical idle and back to L0.



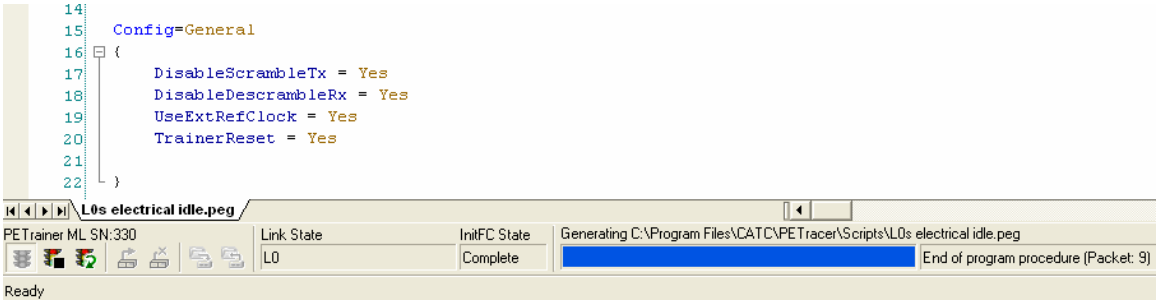
5. In The PE Tracer menu, Resume Traffic Generation. The DUT will transition from L0 to Tx elec_idle state, as shown:



The scope will trigger on the signal and acquire the End of the Electrical Idle Ordered Set



6. To bring the DUT back to L0, just Start Generation to make the Host Emulator transition to L0, as shown:



7. Test complete.

§ § §